

AZ100LVEL16VV

Dual Frequency ECL/PECL Oscillator Gain Stage & Buffer with Enable

FEATURES

- High Bandwidth for $\geq 1\text{GHz}$
- Similar Operation as AZ100EL16VR Except with Selectable Data Input Pairs
- Operating Range of 3.0V to 5.5V
- Minimizes External Components
- Available in a 3x3mm MLP Package
- S-Parameter (.s2p) and IBIS Model Files Available on Arizona Microtek Website
- $>2\text{ kV}$ HBM ESD Protection
- Additional ESD Data Available on Arizona Microtek Website

PACKAGE AVAILABILITY

PACKAGE	PART NUMBER	MARKING	NOTES
MLP 16 (3x3) RoHS Compliant / Lead (Pb) Free	AZ100LVEL16VVL+	AZM+ 16K <Date Code>	1,2

- 1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
- 2 Date code format: "Y" for year followed by "WW" for week.

DESCRIPTION

The AZ100LVEL16VV is a specialized oscillator gain stage with two selectable data input pairs and a high gain output buffer including an enable. The Q_{HG}/\bar{Q}_{HG} outputs have a voltage gain several times greater than the Q/Q outputs.

The AZ100LVEL16VV provides two selectable data input pairs that permit switching between two different oscillator frequencies. When the select pin (SEL) is LOW or open (NC) data from the $D0/\bar{D}0$ is selected. When the SEL pin is HIGH data from the $D1/\bar{D}1$ is selected. Allowing continuous oscillator operation, the (EN) enable works with either data input pair. When EN is HIGH or open (NC), input data is passed to both sets of outputs. When EN is LOW, the Q_{HG}/\bar{Q}_{HG} outputs will be forced LOW/HIGH respectively, while input data will continue to be passed to the Q/Q outputs. The EN and SEL inputs can be driven with an ECL/PECL signal or a full supply swing CMOS type logic signal.

The AZ100LVEL16VV also provides a V_{BB} with a 1.5mA sink/source current. Each data input is separately connected to V_{BB} with a 470Ω internal bias resistor. Bypassing V_{BB} to ground with a $0.01\ \mu\text{F}$ capacitor is recommended.

Each Q/Q output has a 4 mA on-chip pull-down current source. External resistors may also be used to increase pull-down current of the Q/Q to a maximum of 25mA each (includes a 4 mA on-chip current source).

NOTE: Specifications in the ECL/PECL tables are valid when thermal equilibrium is established.

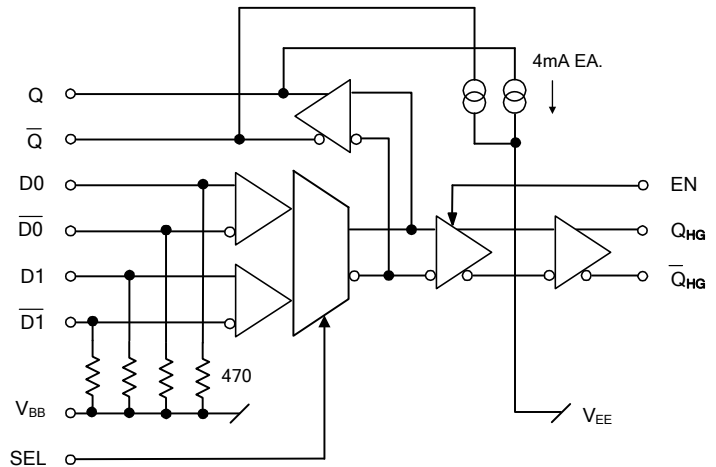
AZ100LVEL16VV

PIN DESCRIPTION

PIN	FUNCTION
D0/D \bar{D} 0, D1/D \bar{D} 1	Data Inputs
Q/Q \bar{Q}	Data Outputs
Q _{HG} /Q \bar{Q} _{HG}	Data Outputs w/High Gain
V _{BB}	Reference Voltage Output
SEL	Selects Data Inputs
EN	Enable Input
V _{CC}	Positive Supply
V _{EE}	Negative Supply

TRUTH TABLE

EN	SEL	Q	Q \bar{Q}	Q _{HG}	Q \bar{Q} _{HG}
High/ Open	Low/ Open	D0/D \bar{D} 0	D0/D \bar{D} 0	D0/D \bar{D} 0	D0/D \bar{D} 0
High/ Open	High	D1/D \bar{D} 1	D1/D \bar{D} 1	D1/D \bar{D} 1	D1/D \bar{D} 1
Low	Low/ Open	D0/D \bar{D} 0	D0/D \bar{D} 0	Low	High
Low	High	D1/D \bar{D} 1	D1/D \bar{D} 1	Low	High



Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V _{CC}	PECL Power Supply (V _{EE} = 0V)	0 to +6.0	Vdc
V _I	PECL Input Voltage (V _{EE} = 0V)	0 to +6.0	Vdc
V _{D/D}	PECL D/D Input Voltage (V _{EE} = 0V)	±0.75 with respect to V _{BB}	Vdc
V _{EE}	ECL Power Supply (V _{CC} = 0V)	-6.0 to 0	Vdc
V _I	ECL Input Voltage (V _{CC} = 0V)	-6.0 to 0	Vdc
V _{D/D}	ECL D/D Input Voltage (V _{CC} = 0V)	±0.75 with respect to V _{BB}	Vdc
I _{OUT}	Output Current --- Continuous Q/Q	25	mA
	--- Surge Q/Q	50	
	--- Continuous Q _{HG} /Q \bar{Q} _{HG}	50	
	--- Surge Q _{HG} /Q \bar{Q} _{HG}	100	
T _A	Operating Temperature Range	-40 to +85	°C
T _{STG}	Storage Temperature Range	-65 to +150	°C

1. This voltage is the difference between each input pin (D/D) and V_{BB}.

ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit	
		Min	Max	Min	Max	Min	Max	Min	Max		
V _{OH}	Output HIGH Voltage ¹	-1045	-835	-1025	-835	-1025	-835	-1025	-835	mV	
V _{OL}	Output LOW Voltage ¹	-1925	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV	
V _{IH}	Input HIGH Voltage	D/D	-1165	-740	-1165	-740	-1165	-740	-1165	-740	mV
		EN, SEL	-1165	V _{CC}	-1165	V _{CC}	-1165	V _{CC}	-1165	V _{CC}	
V _{IL}	Input LOW Voltage	D/D	-1900	-1475	-1900	-1475	-1900	-1475	-1900	-1475	mV
		EN, SEL	V _{EE}	-1475	V _{EE}	-1475	V _{EE}	-1475	V _{EE}	-1475	
V _{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV	
I _{IL}	Input LOW Current EN/SEL	-100		-100		-100		-100		μA	
I _{IH}	Input HIGH Current EN/SEL		150		150		150		150	μA	
I _{EE}	Power Supply Current ¹		47		47		47		51	mA	

1. Specified with Q/Q open and each Q_{HG}/Q \bar{Q} _{HG} output terminated through a 50Ω resistor to V_{CC}-2V.

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LVPECL DC Characteristics ($V_{EE} = \text{GND}$, $V_{CC} = +3.3\text{V}$)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit	
		Min	Max	Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage ^{1,2}	2255	2465	2275	2465	2275	2465	2275	2465	mV	
V_{OL}	Output LOW Voltage ^{1,2}	1375	1745	1400	1680	1400	1680	1400	1680	mV	
V_{IH}	Input HIGH Voltage ¹	D/D	2135	2560	2135	2560	2135	2560	2135	2660	mV
		EN/SEL	2135	V_{CC}	2135	V_{CC}	2135	V_{CC}	2135	V_{CC}	
V_{IL}	Input LOW Voltage ¹	D/D	1050	1825	1050	1825	1050	1825	1050	1825	mV
		EN/SEL	V_{EE}	1825 ¹	V_{EE}	1825	V_{EE}	1825	V_{EE}	1825	
V_{BB}	Reference Voltage ¹	1910	2050	1910	2050	1910	2050	1910	2050	mV	
I_{IL}	Input LOW Current ³ EN/SEL	-400		-400		-400		-500		μA	
I_{IH}	Input HIGH Current EN/SEL		150		150		150		150	μA	
I_{EE}	Power Supply Current		47		47		47		51	mA	

1. Voltage levels vary 1:1 with V_{CC} .
2. Specified with Q/Q open and each Q_{HG}/Q_{HG} output terminated through a 50 Ω resistor to $V_{CC}-2\text{V}$.
3. Specified with EN and SEL forced to V_{EE} .

PECL DC Characteristics ($V_{EE} = \text{GND}$, $V_{CC} = +5.0\text{V}$)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit	
		Min	Max	Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage ^{1,2}	3955	4165	3975	4165	3975	4165	3975	4165	mV	
V_{OL}	Output LOW Voltage ^{1,2}	3075	3445	3100	3380	3100	3380	3100	3380	mV	
V_{IH}	Input HIGH Voltage ¹	D/D	3835	4260	3835	4260	3835	4260	3835	4260	mV
		EN/SEL	3835	V_{CC}	3835	V_{CC}	3835	V_{CC}	3835	V_{CC}	
V_{IL}	Input LOW Voltage ¹	D/D	3100	3525	3100	3525	3100	3525	3100	3525	mV
		EN/SEL	V_{EE}	3525	V_{EE}	3525	V_{EE}	3525	V_{EE}	3525	
V_{BB}	Reference Voltage ¹	3610	3750	3610	3750	3610	3750	3610	3750	mV	
I_{IL}	Input LOW Current ³ EN/SEL	-1000		-1000		-1000		-1200		μA	
I_{IH}	Input HIGH Current EN/SEL		150		150		150		150	μA	
I_{EE}	Power Supply Current		47		47		47		51	mA	

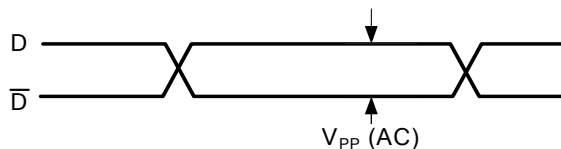
1. Voltage levels vary 1:1 with V_{CC} .
2. Specified with Q/Q open and each Q_{HG}/Q_{HG} output terminated through a 50 Ω resistor to $V_{CC}-2\text{V}$.
3. Specified with EN and SEL forced to V_{EE} .

AC Characteristics ($V_{EE} = -3.0\text{V}$ to -5.5V , $V_{CC} = \text{GND}$ or $V_{EE} = \text{GND}$, $V_{CC} = +3.0\text{V}$ to $+5.5\text{V}$)

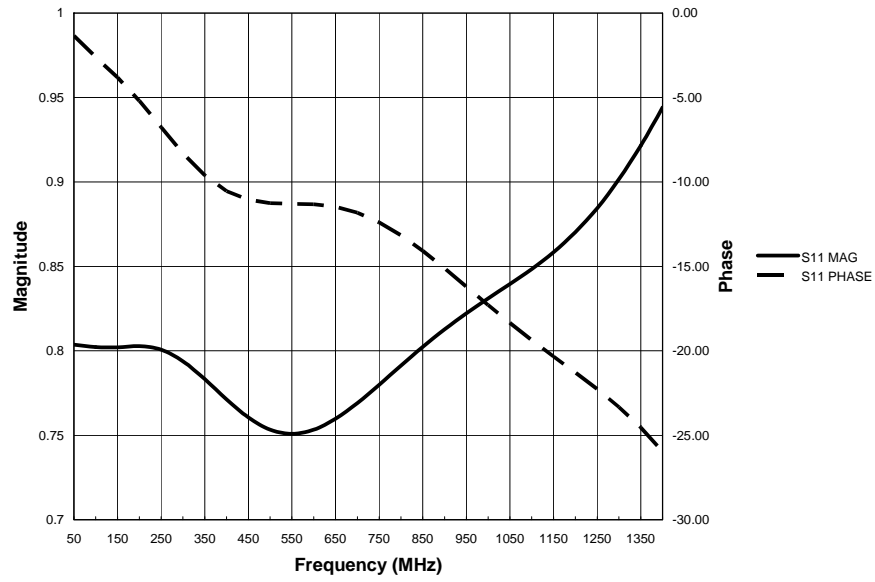
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} / t_{PHL}	Propagation Delay ¹ D to Q/Q Output (SE) D to Q_{HG}/Q_{HG} Outputs (SE)			400			400			400			430	ps
				550			550			550			630	
t_{SKEW}	Duty Cycle Skew ² (SE)		5	20		5	20		5	20		5	20	ps
$V_{PP}(\text{AC})$	Minimum Input Swing ³	80		1000	80		1000	80		1000	80		1000	mV
t_r / t_f	Output Rise/Fall Times ¹ (20% - 80%)	100		260	100		260	100		260	100		260	ps

1. Specified with each output terminated through a 50 Ω resistor to $V_{CC}-2\text{V}$.
2. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
3. V_{PP} is the minimum peak-to-peak input swing for which AC parameters guaranteed. The device has a voltage gain of ≈ 20 to Q/Q outputs and a voltage gain of ≈ 100 to Q_{HG}/Q_{HG} outputs.

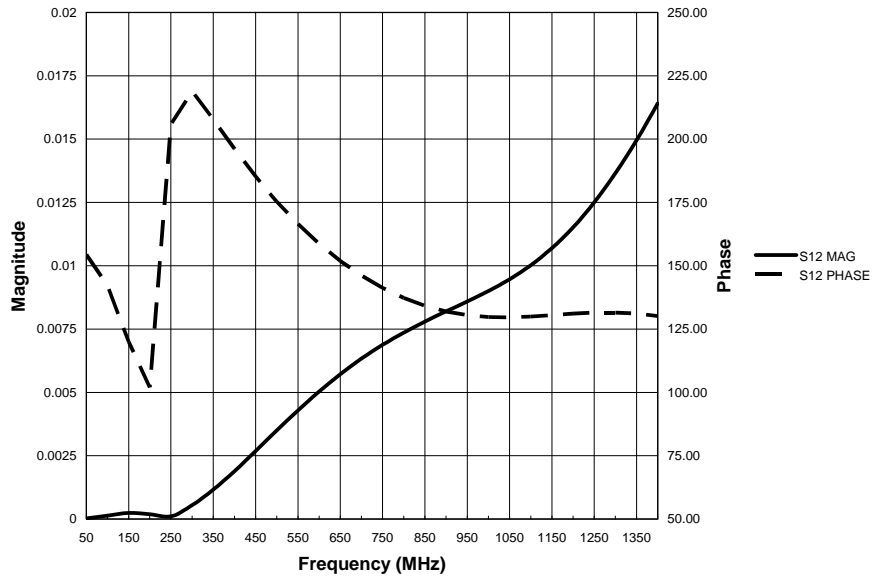
AC PP INPUT



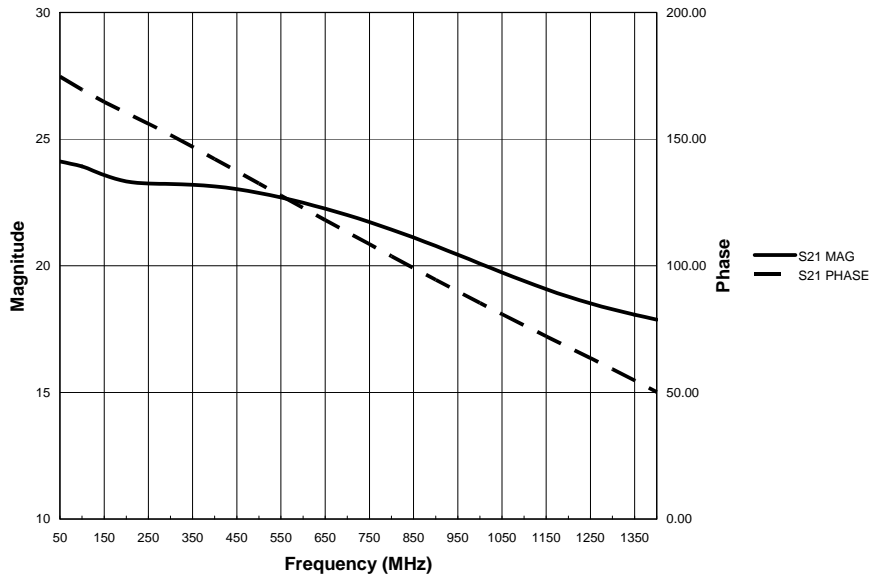
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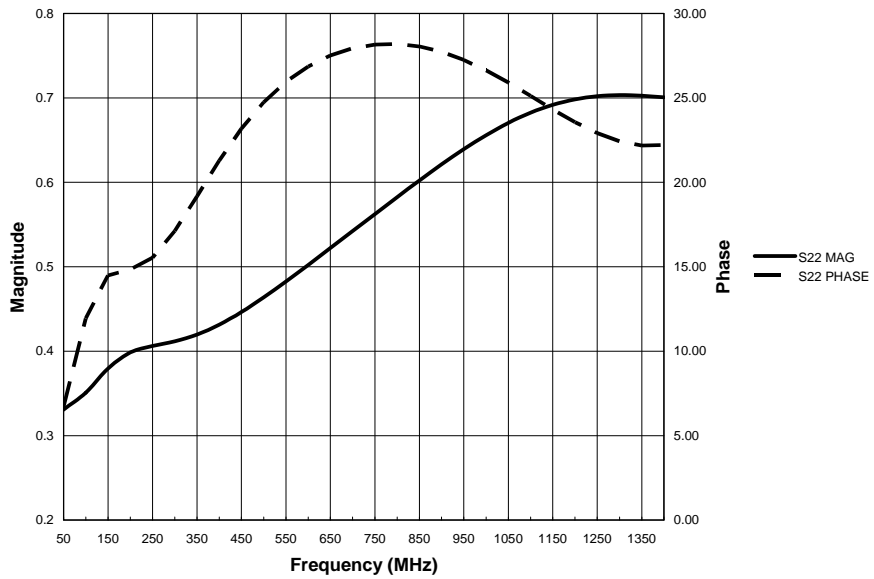
S11, D0/D1 to Q, 50 Ω AC load on Q



S12, D0/D1 to Q, 50 Ω AC load on Q

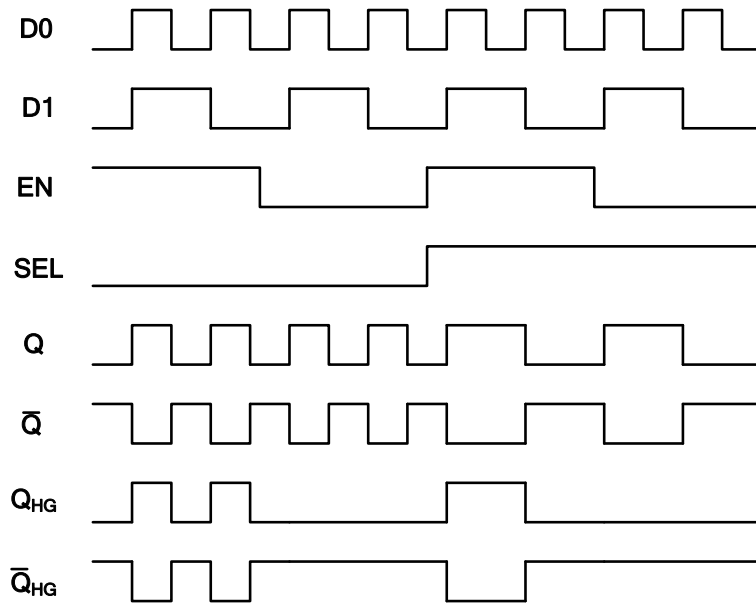


S21, D0/D1 to Q, 50 Ω AC load on Q

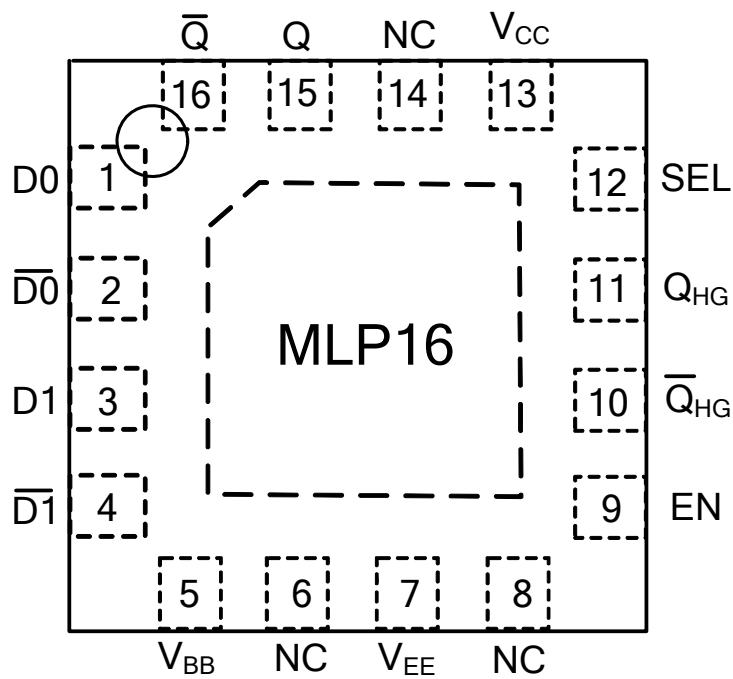


S22, D0/D1 to Q, 50 Ω AC load on Q

TIMING DIAGRAM

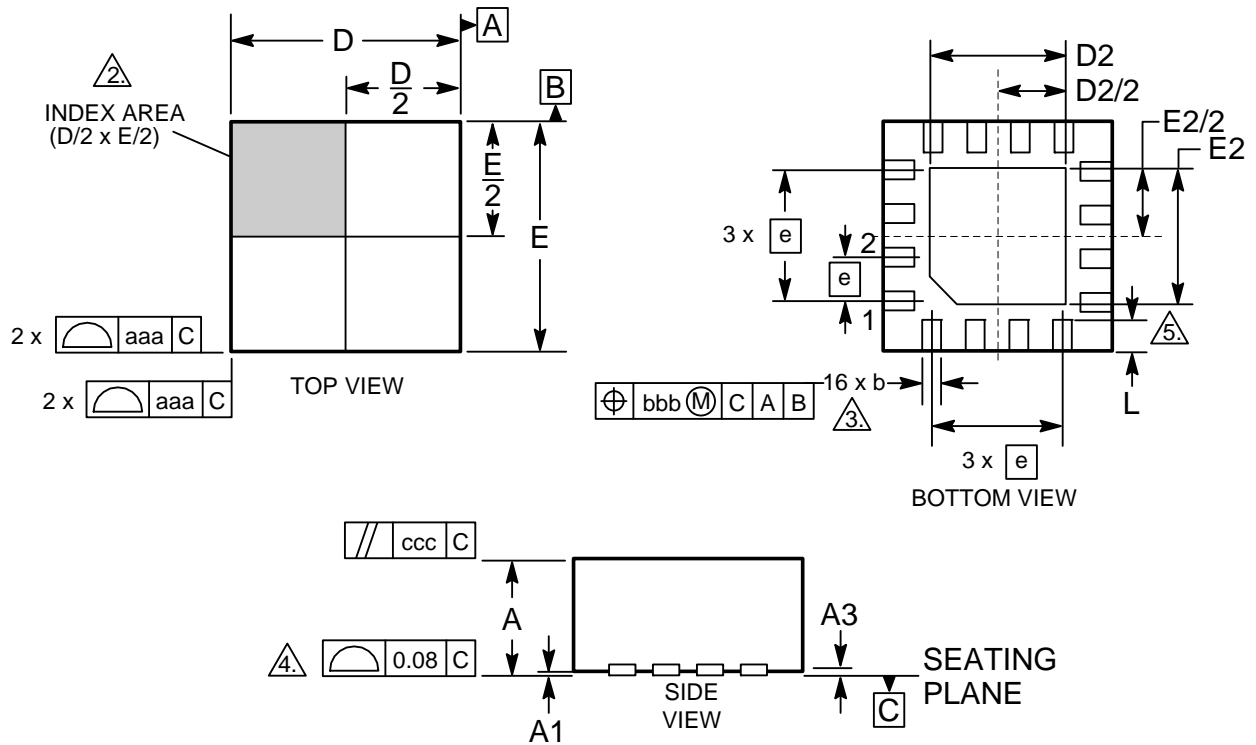


PINOUPS FOR MLP16 PACKAGE



Bottom Center Pad may be left open or tied to V_{EE}

**PACKAGE DIAGRAM
MLP 16**



- NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
 2. THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
 3. DIMENSION b APPLIES TO METALLIZED PAD AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM PAD TIP.
 4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
 5. INSIDE CORNERS OF METALLIZED PAD MAY BE SQUARE OR ROUNDED

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.25 REF	
b	0.18	0.30
D	2.90	3.10
D2	0.25	1.95
E	2.90	3.10
E2	0.25	1.95
e	0.50 BSC	
L	0.30	0.50
aaa	0.25	
bbb	0.10	
ccc	0.10	

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