



AZ100LVEL16VT ARIZONA MICROTEK, INC.

ECL/PECL Oscillator Gain Stage & Buffer with Selectable Enable

FEATURES

- High Bandwidth for $\geq 1\text{GHz}$
- **Similar Operation as AZ100LVEL16VR except in Disabled Condition: Q_{HG} is High**
- -147 dBc/Hz Typical Noise Floor in Oscillator Applications
- Operating Range of 3.0V to 5.5V
- Minimizes External Components
- Selectable Enable Polarity and Threshold (CMOS/TTL or PECL)
- S-Parameter (.s2p) and IBIS Model Files Available on Arizona Microtek Website
- $>2\text{ kV}$ HBM ESD Protection
- Additional ESD Data Available on Arizona Microtek Website

PACKAGE AVAILABILITY

PACKAGE	PART NUMBER	MARKING	NOTES
MLP 8 (2x2x0.75) RoHS Compliant / Lead (Pb) Free	AZ100LVEL16VTNA+	P9+ <Date Code>	1,2
MLP 8 (2x2x0.75) RoHS Compliant / Lead (Pb) Free	AZ100LVEL16VTNB+	P8+ <Date Code>	1,2

- 1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
- 2 Date code format: "Y" or "YY" for year followed by "WW" for week.

DESCRIPTION

The AZ100LVEL16VT is a specialized oscillator gain stage with high gain output buffer including an enable. The Q_{HG}/Q_{HG} outputs have a voltage gain several times greater than the Q output. When the EN input is LOW, the Q and Q_{HG}/Q_{HG} outputs follow the data inputs. When EN is HIGH, the Q_{HG} output is forced high and the Q_{HG} output is forced low.

For the VTNA, both D and D inputs are brought out and tied to the V_{BB} pin through 470Ω internal bias resistors. In the VTNB, the D input is internally tied directly to the V_{BB} pin and the D input is tied to the V_{BB} pin through a 470Ω internal bias resistor. Bypassing V_{BB} to ground with a $0.01\ \mu\text{F}$ capacitor is recommended.

NOTE: Specifications in the ECL/PECL tables are valid when thermal equilibrium is established.

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Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V _{CC}	PECL Power Supply (V _{EE} = 0V)	0 to +6.0	Vdc
V _{D/D}	PECL D/D Input Voltage (V _{EE} = 0V)	±0.75 with respect to V _{BB}	Vdc
V _{EN}	PECL EN Input Voltage (V _{EE} = 0V)	0 to +6.0	Vdc
V _{EE}	ECL Power Supply (V _{CC} = 0V)	-6.0 to 0	Vdc
V _{D/D}	ECL D/D Input Voltage (V _{CC} = 0V)	±0.75 with respect to V _{BB}	Vdc
V _{EN}	ECL EN Input Voltage (V _{CC} = 0V)	-6.0 to 0	Vdc
I _{OUT}	Output Current, Q/Q — Continuous — Surge	25 50	mA
I _{HGOUT}	Output Current, Q _{HG} /Q _{HG} — Continuous — Surge	50 100	mA
T _A	Operating Temperature Range	-40 to +85	°C
T _{STG}	Storage Temperature Range	-65 to +150	°C

ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH}	Output HIGH Voltage ¹	-1045	-835	-1025	-835	-1025	-835	-1025	-835	mV
V _{OL}	Output LOW Voltage ¹	-1925	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V _{IH}	Input HIGH Voltage D/D, EN	-1165	-740	-1165	-740	-1165	-740	-1165	-740	mV
V _{IL}	Input LOW Voltage D/D, EN	-1900	-1475	-1900	-1475	-1900	-1475	-1900	-1475	mV
V _{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I _{IH}	Input HIGH Current EN		150		150		150		150	µA
I _{IL}	Input LOW Current EN	0.5		0.5		0.5		0.5		µA
I _{EE}	Power Supply Current ¹		48		48		48		54	mA

1. Q_{HG}/Q_{HG} terminated through 50Ω resistors to V_{CC} - 2V.

LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	2255	2465	2275	2465	2275	2465	2275	2465	mV
V _{OL}	Output LOW Voltage ^{1,2}	1375	1745	1400	1680	1400	1680	1400	1680	mV
V _{IH}	Input HIGH Voltage ¹ D/D, EN	2135	2560	2135	2560	2135	2560	2135	2560	mV
V _{IL}	Input LOW Voltage ¹ D/D, EN	1400	1825	1400	1825	1400	1825	1400	1825	mV
V _{BB}	Reference Voltage ¹	1910	2050	1910	2050	1910	2050	1910	2050	mV
I _{IH}	Input HIGH Current EN		150		150		150		150	µA
I _{IL}	Input LOW Current EN	0.5		0.5		0.5		0.5		µA
I _{EE}	Power Supply Current ²		48		48		48		54	mA

1. For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.

2. Q_{HG}/Q_{HG} terminated through 50Ω resistors to V_{CC} - 2V.

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PECL DC Characteristics ($V_{EE} = \text{GND}$, $V_{CC} = +5.0\text{V}$)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage ^{1,2}	3955	4165	3975	4165	3975	4165	3975	4165	mV
V_{OL}	Output LOW Voltage ^{1,2}	3075	3445	3100	3380	3100	3380	3100	3380	mV
V_{IH}	Input HIGH Voltage ¹ D/D, EN	3835	4260	3835	4260	3835	4260	3835	4260	mV
V_{IL}	Input LOW Voltage ¹ D/D, EN	3100	3525	3100	3525	3100	3525	3100	3525	mV
V_{BB}	Reference Voltage ¹	3610	3750	3610	3750	3610	3750	3610	3750	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	μA
I_{IL}	Input LOW Current EN	0.5		0.5		0.5		0.5		μA
I_{EE}	Power Supply Current ²		48		48		48		54	mA

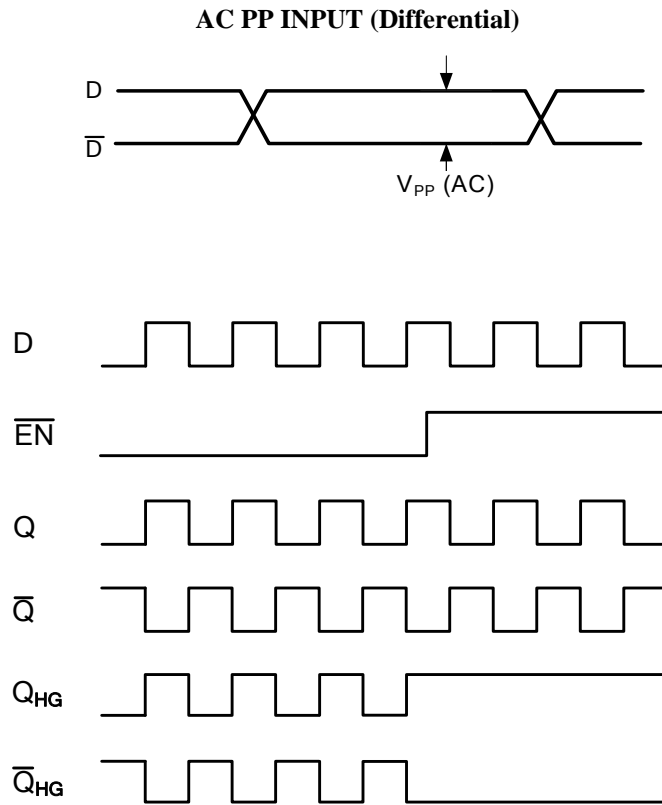
- For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
- Q_{HG}/Q_{HG} terminated through 50Ω resistors to $V_{CC} - 2V$.

AC Characteristics ($V_{EE} = -3.0\text{V}$ to -5.5V ; $V_{CC} = \text{GND}$ or $V_{EE} = \text{GND}$; $V_{CC} = +3.0\text{V}$ to $+5.5\text{V}$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} / t_{PHL}	Propagation Delay D to Q Output ¹ D to Q_{HG}/Q_{HG} Outputs ² (SE)			350 450			350 450			350 450			350 450	ps
t_{SKEW}	Duty Cycle Skew ³ (SE)		5	20		5	20		5	20		5	20	ps
V_{PP}	Input Swing ⁴ Differential (D/D) Single Ended (D, D)	80 160		1000 1500	80 160		1000 1500	80 160		1000 1500	80 160		1000 1500	mV
t_r / t_f	Output Rise/Fall Times ^{1,2} (20% - 80%)	100		240	100		240	100		240	100		240	ps

- Q output specified with 50Ω termination to $V_{CC} - 2V$.
- Q_{HG}/Q_{HG} terminated through 50Ω resistors to $V_{CC} - 2V$.
- Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
- The peak-to-peak input swing is the range for which AC parameters are guaranteed. D and D must remain within the range of ± 750 mV with respect to V_{BB} . The device has a voltage gain of ≈ 20 to the Q outputs and a voltage gain of ≈ 100 to the Q_{HG}/Q_{HG} outputs.

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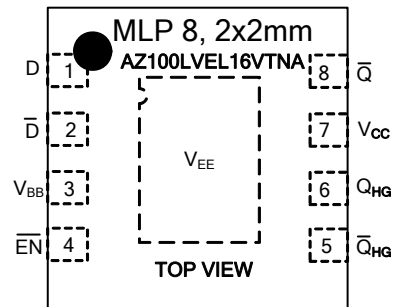
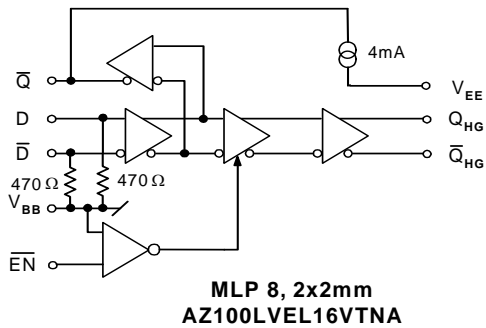


TIMING DIAGRAM

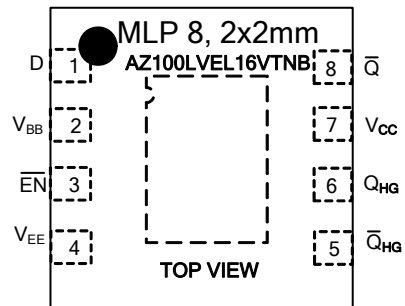
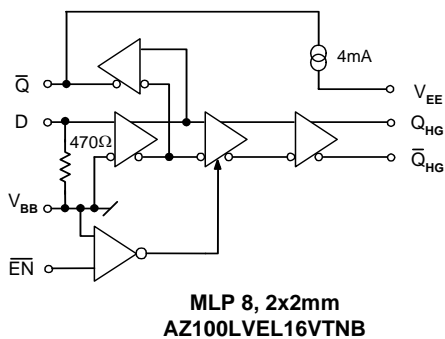
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PIN DESCRIPTIONS

PIN	FUNCTION
D/D	Data Inputs
Q	Data Output
Q _{HG} /Q _{HG}	Data Outputs w/High Gain
V _{BB}	Reference Voltage Output
EN	Enable Input
V _{EE}	Negative Supply
V _{CC}	Positive Supply

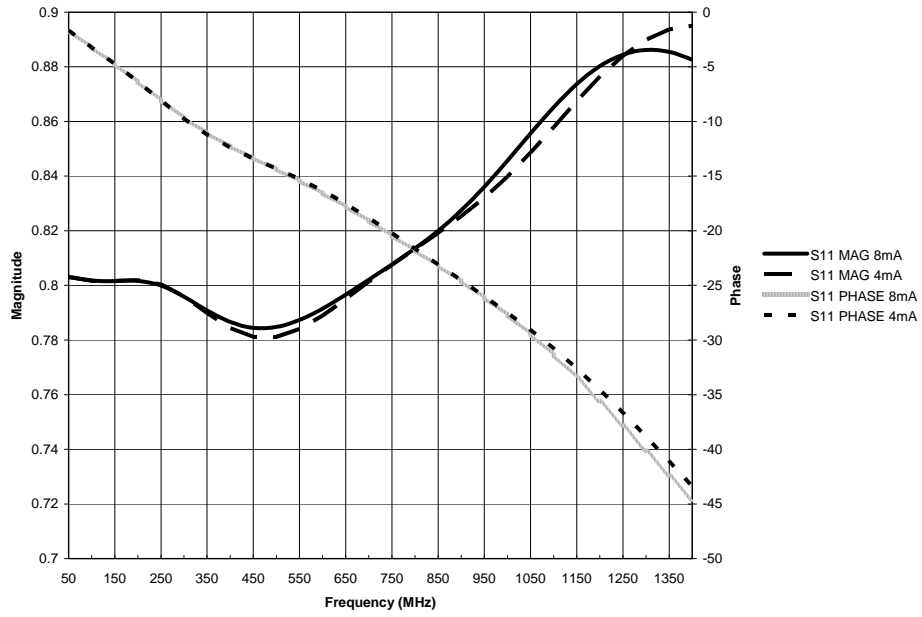


Bottom Center Pad is the V_{EE} return.

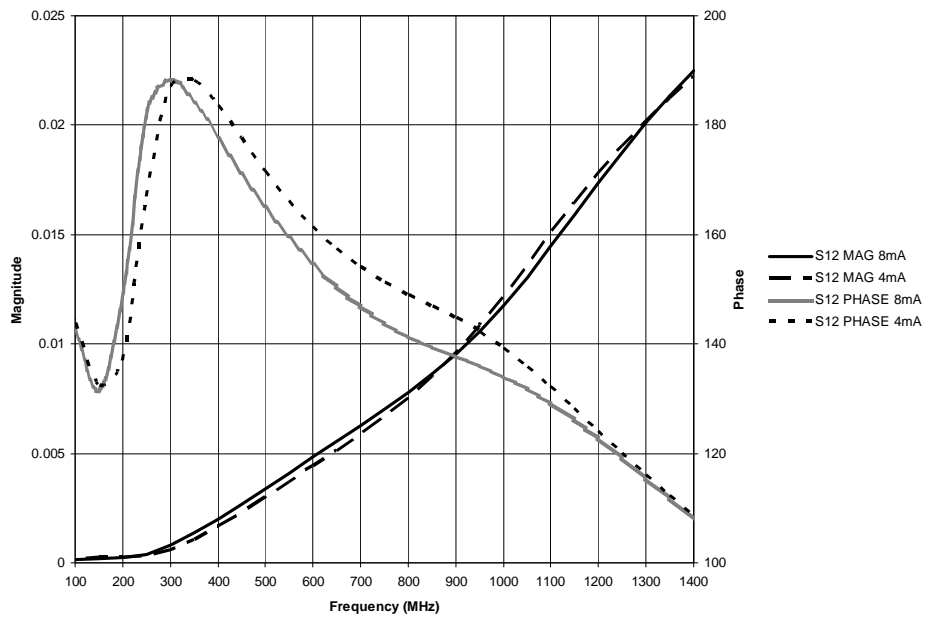


Bottom Center Pad may be left open or tied to V_{EE}. Pin 4 is the V_{EE} return.

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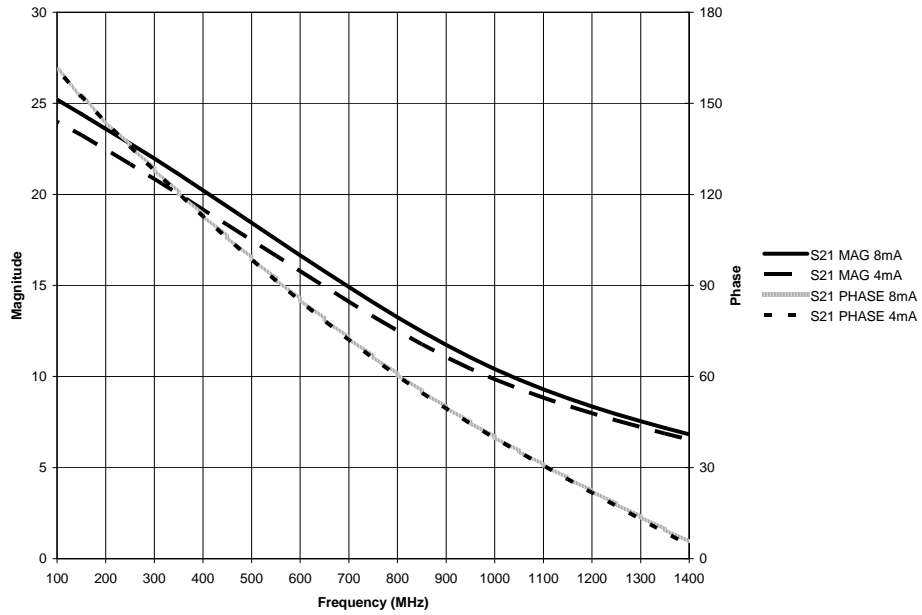


S11, D to Q
(50 Ω external AC, 4 & 8mA internal DC Load on Q)

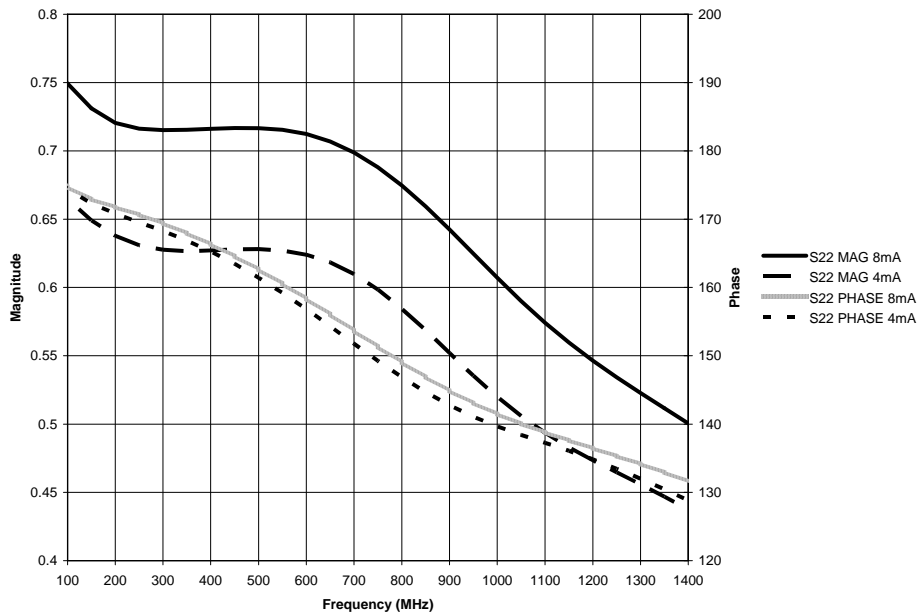


S12, D to Q
(50 Ω external AC, 4 & 8mA internal DC Load on Q)

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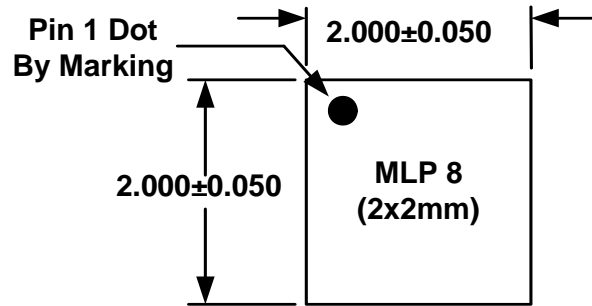


S21, D to Q
(50 Ω external AC, 4 & 8mA internal DC Load on Q)

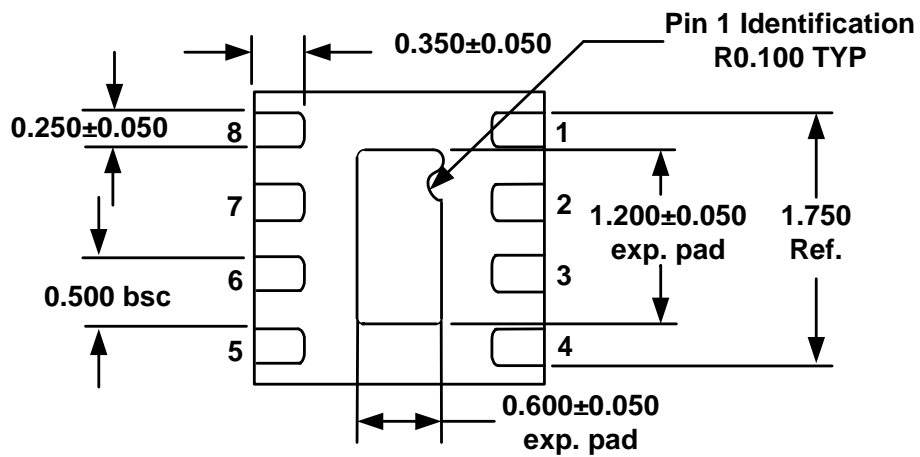


S22, D to Q
(50 Ω external AC, 4 & 8mA internal DC Load on Q)

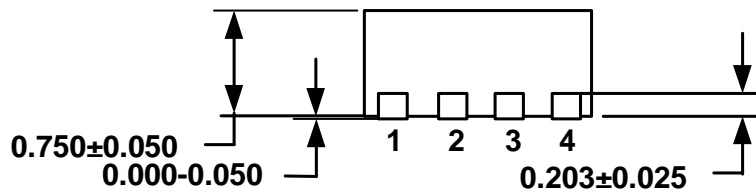
PACKAGE DIAGRAM
MLP 8 2x2mm



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Note: All dimensions are in mm

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