

AZ100ELT21

Differential PECL to CMOS/TTL Translator

FEATURES

- Green / RoHS Compliant / Lead (Pb) Free Package Available
- 3.5ns Typical Propagation Delay
- Differential PECL Inputs
- CMOS/TTL Outputs
- Flow Through Pinouts
- Operating Range of 3.0V to 5.5V
- Direct Replacement for ON Semiconductor MC100ELT21

PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING	NOTES
SOIC 8 Green / RoHS Compliant / Lead (Pb) Free	AZ100ELT21DG	AZM100G ELT21 <Date Code>	1,2
MSOP 8 Green / RoHS Compliant / Lead (Pb) Free	AZ100ELT21TG	AZHG T21 <Date Code>	1,2

- 1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
- 2 Date code format: "Y" for year followed by "WW" for week.

DESCRIPTION

The AZ100ELT21 is a differential PECL to CMOS/TTL translator. Because PECL (Positive ECL) levels are used, only V_{CC} and ground are required. The small outline 8-lead packaging and the single gate of the ELT21 makes it ideal for those applications where space, performance and low power are at a premium.

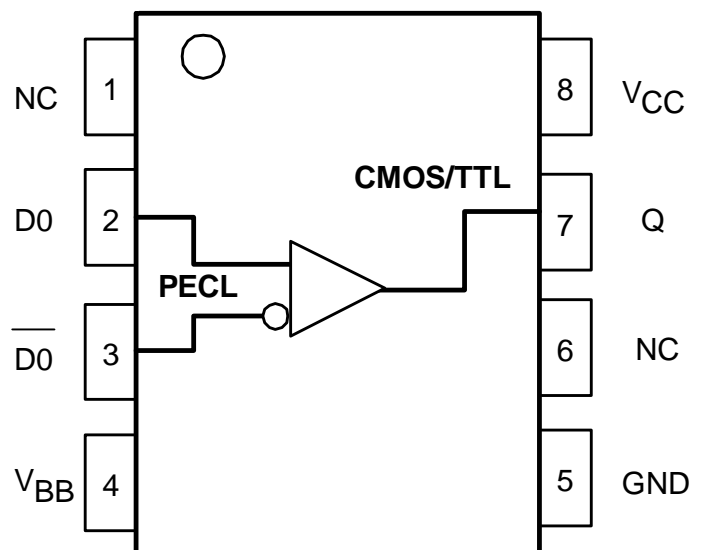
The ELT21 provides a V_{BB} output for single-ended use or a DC bias reference for AC coupling to the device. For single-ended input applications, the V_{BB} reference should be connected to one side of the D0/D0 differential input pair. The input signal is then fed to the other D0/D0 input. The V_{BB} pin should be used only as a bias for the ELT21 as its sink/source capability is limited. When used, the V_{BB} pin should be bypassed to ground via a 0.01 μ F capacitor.

NOTE: Specifications in the ECL/PECL tables are valid when thermal equilibrium is established.

PIN DESCRIPTION

PIN	FUNCTION
Q	CMOS/TTL Output
D0, D0	Differential Inputs
V_{CC}	Positive Supply
V_{BB}	Reference Voltage Output
GND	Ground
NC	No Connect

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



AZ100ELT21

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Character	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	7.0	V
T _A	Operating Temperature Range (In Free-Air)	-40 to +85	°C
T _{STG}	Storage Temperature Range	-65 to +150	°C

CMOS/TTL DC CHARACTERISTICS (V_{CC} = +3.0V to +5.5V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V _{OH}	Output HIGH Voltage	V _{CC} - 0.5			V	I _{OH} = -24 mA
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 24 mA
I _{CC}	Power Supply Current		9.0	15	mA	0°C to 85°C
I _{CC}	Power Supply Current		9.0	17.6	mA	-40°C to 85°C
I _{OS}	Output Short Circuit Current		100		mA	

100K LVPECL DC Characteristics (V_{CC} = +3.3V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	2135		2420	mV
V _{IL}	Input LOW Voltage	1490		1825	1490		1825	1490		1825	1490		1825	mV
V _{BB}	Reference Voltage	1920		2090	1920		2090	1920		2090	1920		2090	mV
V _{PP}	Minimum Input Swing ¹	200			200			200			200			mV
V _{CMR}	Common Mode Range	1.2		V _{CC}	1.2		V _{CC}	1.2		V _{CC}	1.2		V _{CC}	V
I _{IL}	Input LOW Current	0.5			0.5			0.5			0.5			μA
I _{IH}	Input HIGH Current			150						150				μA

1. 200mV input guarantees full logic swing at the output.

100K PECL DC Characteristics (V_{CC} = +5.0V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{IH}	Input HIGH Voltage	3835		4120	3835		4120	3835		4120	3835		4120	mV
V _{IL}	Input LOW Voltage	3190		3525	3190		3525	3190		3525	3190		3525	mV
V _{BB}	Reference Voltage	3620		3790	3620		3790	3620		3790	3620		3790	mV
V _{PP}	Minimum Input Swing ¹	200			200			200			200			mV
V _{CMR}	Common Mode Range	1.2		V _{CC}	1.2		V _{CC}	1.2		V _{CC}	1.2		V _{CC}	V
I _{IL}	Input LOW Current	0.5			0.5			0.5			0.5			μA
I _{IH}	Input HIGH Current			150						150				μA

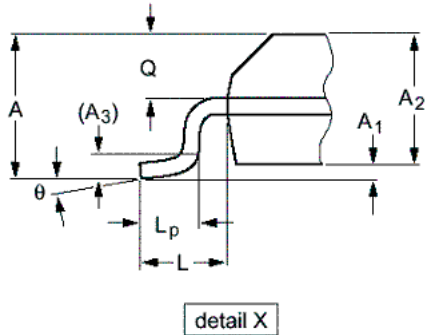
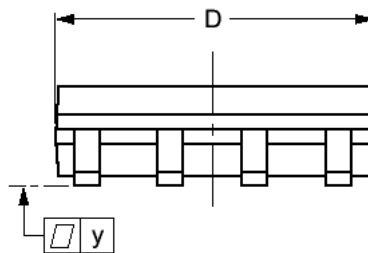
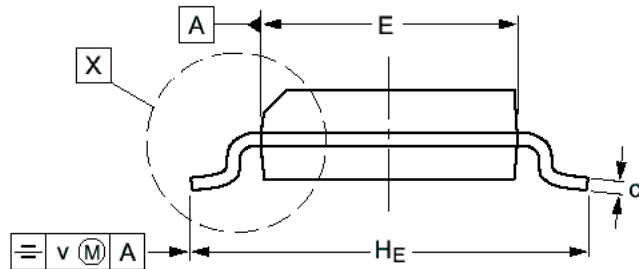
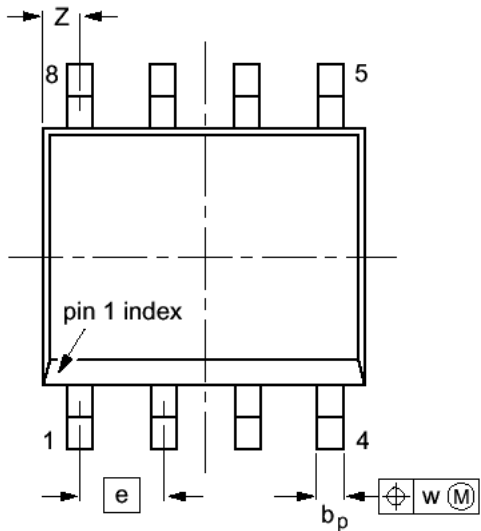
1. 200mV input guarantees full logic swing at the output.

AC Characteristics (V_{CC} = +3.0V to +5.5V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{PLH} / t _{PHL}	Propagation Delay to Output ¹ V _{CC} = 4.5V to 5.5V V _{CC} = 3.0V to 3.6V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	ns
		3.5		7.0	3.5		7.0	3.5		7.0	3.5		7.0	

1. C_L=20pF

**PACKAGE DIAGRAM
SOIC 8**

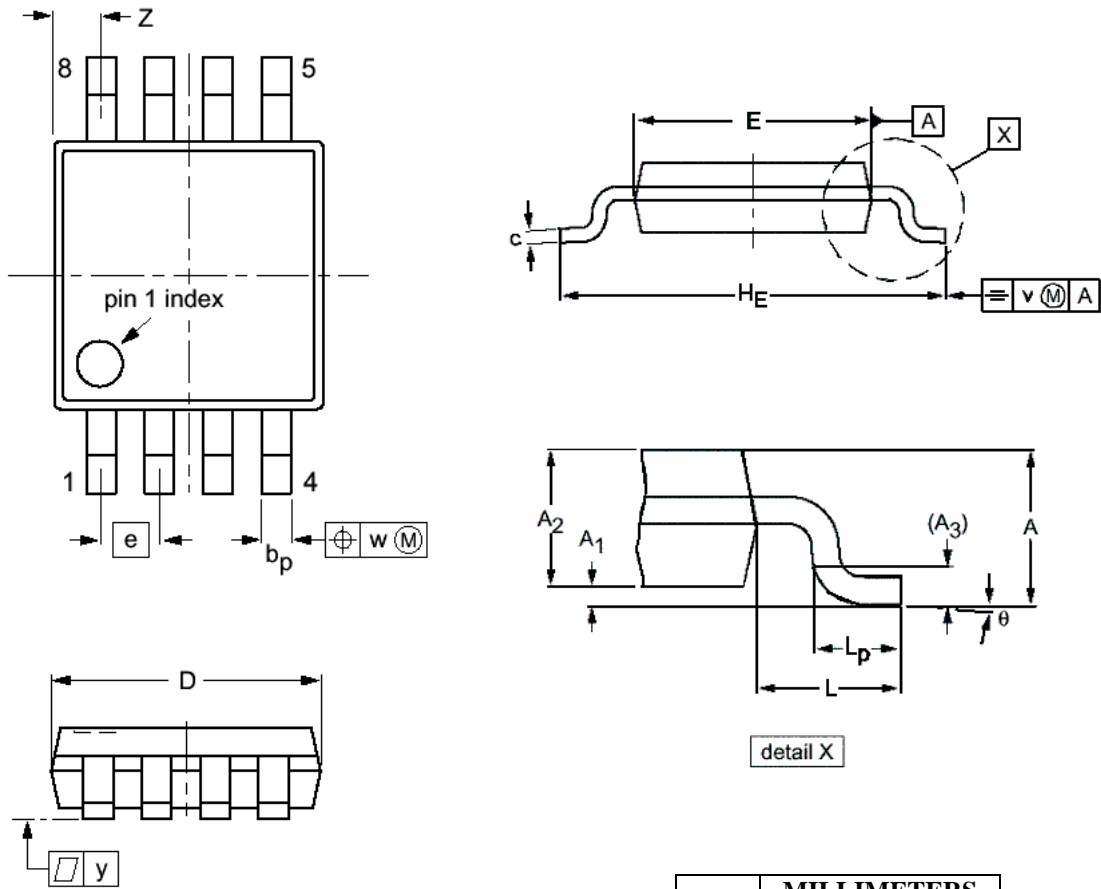


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.25	0.004	0.010
A ₂	1.28	1.57	0.050	0.062
A ₃	0.25		0.01	
b _p	0.36	0.49	0.014	0.019
c	0.19	0.25	0.0075	0.0100
D	4.80	5.00	0.19	0.20
E	3.80	4.00	0.15	0.16
e	1.27		0.050	
H _E	5.80	6.20	0.228	0.244
L	1.05		0.041	
L _p	0.40	1.27	0.016	0.050
Q	0.60	0.70	0.024	0.028
v	0.25		0.01	
w	0.25		0.01	
y	0.10		0.004	
Z	0.30	0.70	0.012	0.028
θ	0°	8°	0°	8°

NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

**PACKAGE DIAGRAM
MSOP 8**



- NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
 3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

DIM	MILLIMETERS	
	MIN	MAX
A		1.10
A ₁	0.05	0.15
A ₂	0.75	0.95
A ₃	0.25	
b _p	0.22	0.40
c	0.13	0.23
D	2.90	3.10
E	2.90	3.10
e	0.65	
H _E	4.75	5.05
L	0.95	
L _p	0.40	0.70
v	0.10	
w	0.08	
y	0.10	
Z	0.38	0.64
θ	0°	6°

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