

AZP92

ECL/PECL $\div 1$, $\div 2$ Clock Generation Chip with Selectable Enable

FEATURES

- Green and RoHS Compliant / Lead (Pb) Free Package Available
- 3.0V to 5.5V Operation
- Selectable Divide Ratio
- Selectable Enable Polarity and Threshold (CMOS/TTL or PECL)
- Selectable Input Biasing
- High Bandwidth, 1.5+ GHz ($\div 1$), 3+ GHz ($\div 2$)
- -145 dBc/Hz ($\div 1$), -151 dBc/Hz ($\div 2$) Typical Noise Floor
- Available in a MLP 8 (2x2) Package
- S Parameter and IBIS Model Files Available on Arizona Microtek Website
- >2 kV HBM ESD Protection
- Additional ESD Data Available on Arizona Microtek Website

PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING	NOTES
MLP 8 (2x2) Green / RoHS Compliant / Lead (Pb) Free	AZP92NAG	P1G <Date Code>	1,2

- 1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
- 2 Date code format: "Y" for year followed by "WW" for week.

DESCRIPTION

The AZP92 is a specialized $\div 1$ or $\div 2$ clock generation part including an enable/reset function. The divide ratio is selected with the DIV-SEL pin/pad. When DIV-SEL is open (NC), the AZP92 functions as a standard receiver. If DIV-SEL is connected to V_{EE} , it functions as a $\div 2$ divider.

A selectable enable is provided which also functions as a reset when the $\div 2$ mode is selected. Enable (EN) functionality is selected with the EN-SEL pin/pad which has three valid states: open (NC), V_{EE} , or connected to V_{EE} via a 20k Ω resistor. Leaving EN-SEL open or connecting it to V_{EE} will select the EN pin/pad to function as an active high CMOS/TTL enable. When EN-SEL is open, an internal 75k Ω pull-up resistor is selected which enables the outputs whenever EN is left open. When EN-SEL is connected to V_{EE} , an internal 75k Ω pull-down resistor is selected which disables the outputs whenever EN is left open.

Connecting the EN-SEL to V_{EE} with a 20k Ω resistor will select the EN pin/pad to function as an active low PECL/ECL enable with an internal 75k Ω pull-down resistor. In this mode, outputs are enabled when EN is left open (NC). This default logic condition can be overridden by connecting the EN to V_{CC} with an external resistor of $\leq 20k\Omega$. Refer to the enable truth table on the next page for detailed operation.

MLP 8, 2x2 mm Package (AZP92NA)

The AZP92NA provides a V_{BB} with an 1880 Ω internal bias resistor from D to V_{BB} . This feature allows AC coupling with minimal external components. The V_{BB} pin supports 1.5mA sink/source current and should be bypassed to ground or V_{CC} with a 0.01 μ F capacitor.

NOTE: The specifications in the ECL/PECL tables are valid when thermal equilibrium has been established.

SIGNAL DESCRIPTION

PIN/PAD	FUNCTION
D	Data Input
Q/Q	Data Outputs
V _{BB} /D	Reference Voltage Output
EN	Enable/Reset Input
EN-SEL	Enable Logic Select
DIV-SEL	Divide Ratio Select
V _{EE}	Negative Supply
V _{CC}	Positive Supply

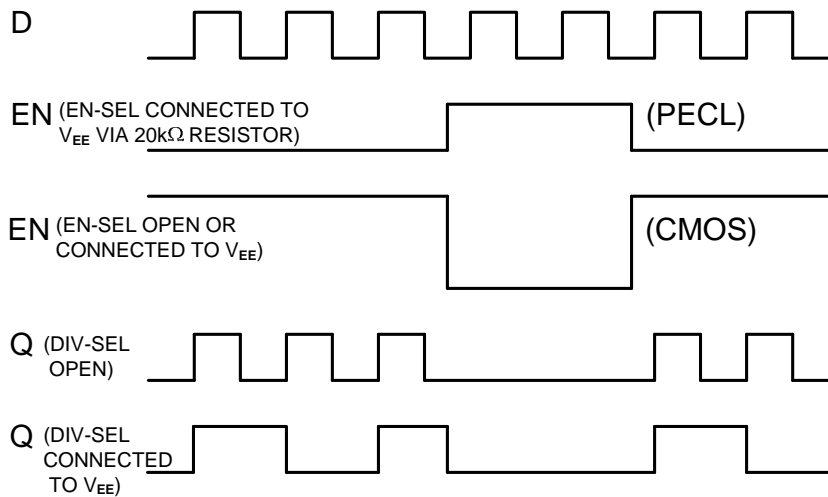
ENABLE TRUTH TABLE

EN-SEL	EN	Q	Q
NC	CMOS Low or V _{EE}	Low	High
NC	CMOS High, V _{CC} or NC	Data	Data
V _{EE}	CMOS Low, V _{EE} or NC	Low	High
V _{EE}	CMOS High or V _{CC}	Data	Data
20kΩ to V _{EE}	PECL Low, V _{EE} or NC	Data	Data
20kΩ to V _{EE}	PECL High or V _{CC}	Low	High

DIVIDE TRUTH TABLE

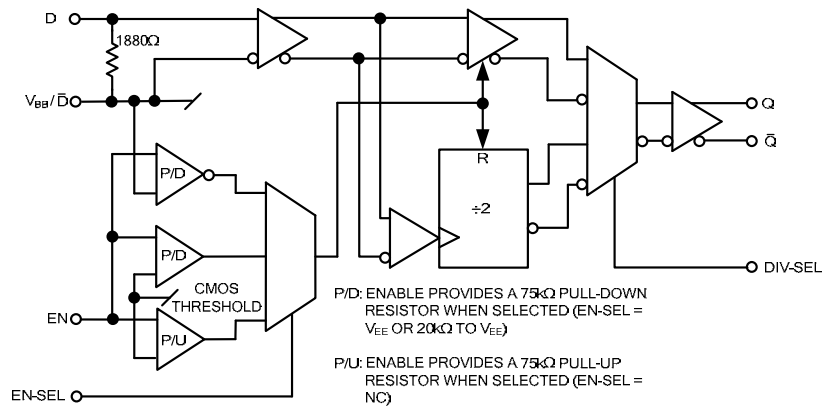
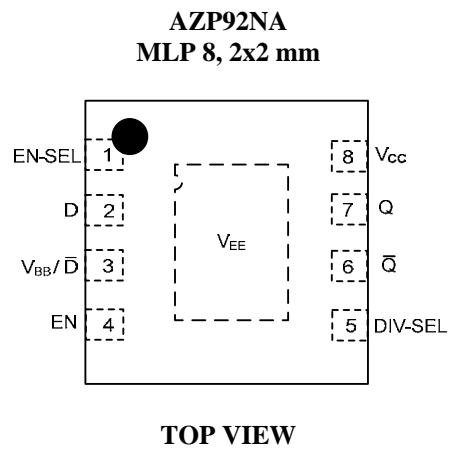
DIV-SEL	DIVIDE RATIO
NC	÷1
V _{EE} ¹	÷2

¹ DIV-SEL connection must be ≤1Ω.



TIMING DIAGRAM

AZP92



Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V _{CC}	PECL Power Supply (V _{EE} = 0V)	0 to +6.0	Vdc
V _I	PECL Input Voltage (V _{EE} = 0V)	0 to +6.0	Vdc
V _{EE}	ECL Power Supply (V _{CC} = 0V)	-6.0 to 0	Vdc
V _I	ECL Input Voltage (V _{CC} = 0V)	-6.0 to 0	Vdc
I _{HGOUT}	Output Current — Continuous — Surge	50 100	mA
T _A	Operating Temperature Range	-40 to +85	°C
T _{STG}	Storage Temperature Range	-65 to +150	°C

100K ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH}	Output HIGH Voltage ¹	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
V _{OL}	Output LOW Voltage ¹	-1900	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V _{IH}	Input HIGH Voltage D/D, EN (ECL) ² EN (CMOS) ³	-1165 V _{EE} +2000	-390 V _{CC}	-1165 V _{EE} +2000	-390 V _{CC}	-1165 V _{EE} +2000	-390 V _{CC}	-1165 V _{EE} +2000	-390 V _{CC}	mV
V _{IL}	Input LOW Voltage D/D, EN (ECL) ² EN (CMOS) ³	-2250 V _{EE}	-1475 V _{EE} + 800	-2250 V _{EE}	-1475 V _{EE} + 800	-2250 V _{EE}	-1475 V _{EE} + 800	-2250 V _{EE}	-1475 V _{EE} + 800	mV
V _{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I _{IH}	Input HIGH Current EN		150		150		150		150	µA
I _{IL}	Input LOW Current EN (ECL) ² EN (CMOS) ³	0.5 -150		0.5 -150		0.5 -150		0.5 -150		µA
I _{EE}	Power Supply Current ⁴		31		31		31		34	mA

1. Specified with outputs terminated through 50Ω resistors to V_{CC} - 2V.
2. EN-SEL connected to V_{EE} through a 20kΩ resistor.
3. EN-SEL connected V_{EE} or left open (NC).
4. DIV-SEL left open (NC).

100K LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	2215	2420	2275	2420	2275	2420	2275	2420	mV
V _{OL}	Output LOW Voltage ^{1,2}	1400	1745	1400	1680	1400	1680	1400	1680	mV
V _{IH}	Input HIGH Voltage ¹ D/D, EN (PECL) ³ EN (CMOS) ⁴	2135 2000	2910 V _{CC}	2135 2000	2910 V _{CC}	2135 2000	2910 V _{CC}	2135 2000	2910 V _{CC}	mV
V _{IL}	Input LOW Voltage ¹ D/D, EN (PECL) ³ EN (CMOS) ⁴	1050 GND	1825 800	1050 GND	1825 800	1050 GND	1825 800	1050 GND	1825 800	mV
V _{BB}	Reference Voltage ¹	1910	2050	1910	2050	1910	2050	1910	2050	mV
I _{IH}	Input HIGH Current EN		150		150		150		150	µA
I _{IL}	Input LOW Current EN (PECL) ³ EN (CMOS) ⁴	0.5 -150		0.5 -150		0.5 -150		0.5 -150		µA
I _{EE}	Power Supply Current ⁵		31		31		31		34	mA

1. For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.
2. Specified with outputs terminated through 50Ω resistors to V_{CC} - 2V.
3. EN-SEL connected to V_{EE} through a 20kΩ resistor.
4. EN-SEL connected V_{EE} or left open (NC).
5. DIV-SEL left open (NC).

100K PECL DC Characteristics ($V_{EE} = \text{GND}$, $V_{CC} = +5.0\text{V}$)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage ^{1,2}	3915	4120	3975	4120	3975	4120	3975	4120	mV
V_{OL}	Output LOW Voltage ^{1,2}	3100	3445	3100	3380	3100	3380	3100	3380	mV
V_{IH}	Input HIGH Voltage ¹	3835	4610	3835	4610	3835	4610	3835	4610	mV
	D/D, EN (PECL) ³ EN (CMOS) ⁴	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	
V_{IL}	Input LOW Voltage ¹	2750	3525	2750	3525	2750	3525	2750	3525	mV
	D/D, EN (PECL) ³ EN (CMOS) ⁴	GND	800	GND	800	GND	800	GND	800	
V_{BB}	Reference Voltage ¹	3610	3750	3610	3750	3610	3750	3610	3750	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	μA
I_{IL}	Input LOW Current									μA
	EN (PECL) ³ EN (CMOS) ⁴	0.5 -150		0.5 -150		0.5 -150		0.5 -150		
I_{EE}	Power Supply Current ⁵		31		31		31		34	mA

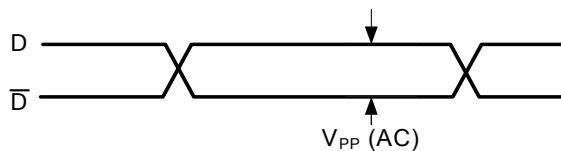
1. For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
2. Specified with outputs terminated through 50Ω resistors to $V_{CC} - 2\text{V}$.
3. EN-SEL connected to V_{EE} through a 20kΩ resistor.
4. EN-SEL connected V_{EE} or left open (NC).
5. DIV-SEL left open (NC).

AC Characteristics ($V_{EE} = -3.0\text{V}$ to -5.5V ; $V_{CC} = \text{GND}$ or $V_{EE} = \text{GND}$; $V_{CC} = +3.0\text{V}$ to $+5.5\text{V}$)

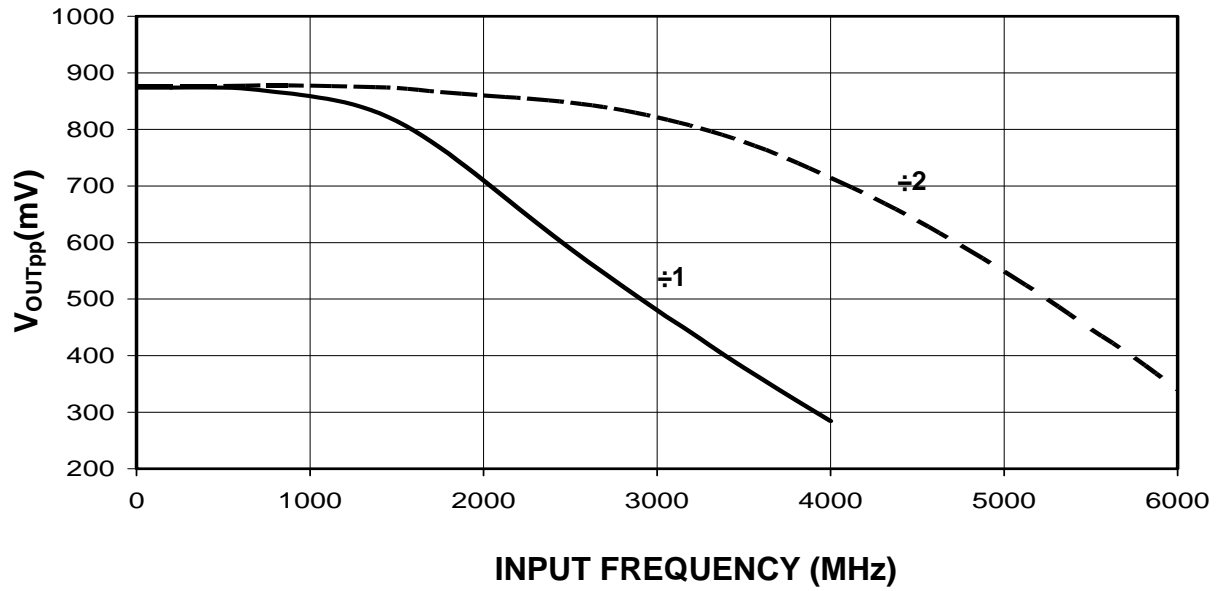
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} / t_{PHL}	Propagation Delay			450			450			450			450	ps
	D to Q/Q Outputs ¹ (SE) EN to Q/Q Outputs ¹			600			600			600			600	
t_{SKEW}	Duty Cycle Skew ² (SE)		5	20		5	20		5	20		5	20	ps
$V_{PP}(\text{AC})$	Input Swing ³			1000			1000			1000			1000	mV
	Differential (D/D) Single Ended (D) ⁴	150 300		2000	150 300		2000	150 300		2000	150 300		2000	
t_r / t_f	Output Rise/Fall ¹ (20% - 80%)	80		200	80		200	80		200	80		200	ps

1. Specified with outputs terminated through 50Ω resistors to $V_{CC} - 2\text{V}$.
2. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
3. The peak-to-peak input swing is the range for which AC parameters are guaranteed.
4. Range valid for AC coupled signals only.

AC PP INPUT (Differential)

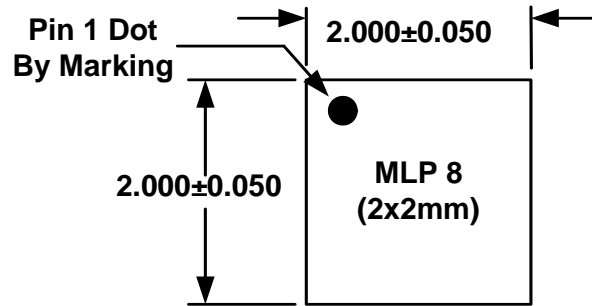


Typical Large Signal Output Swing, Q/Q

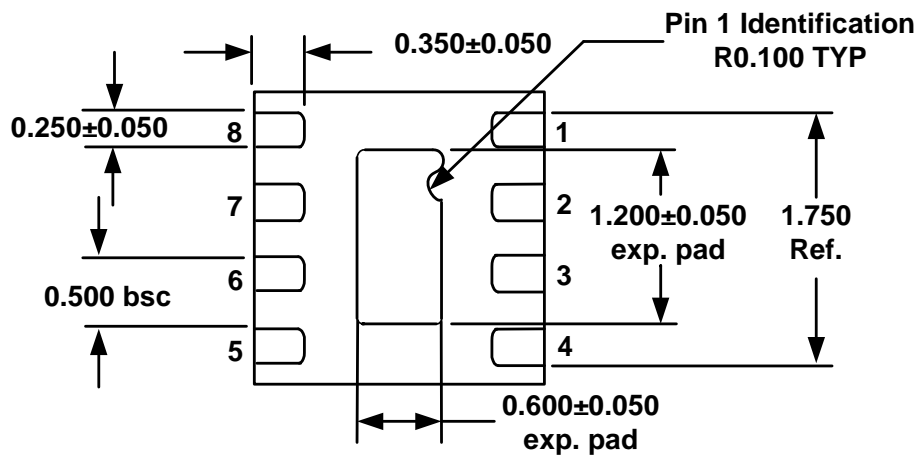


Measured with 750mv D input, Q/Q each terminated to V_{CC}-2V via 50 Ω resistors.

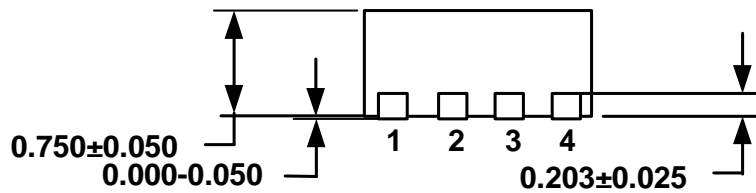
PACKAGE DIAGRAM
MLP 8 2x2mm



TOP VIEW



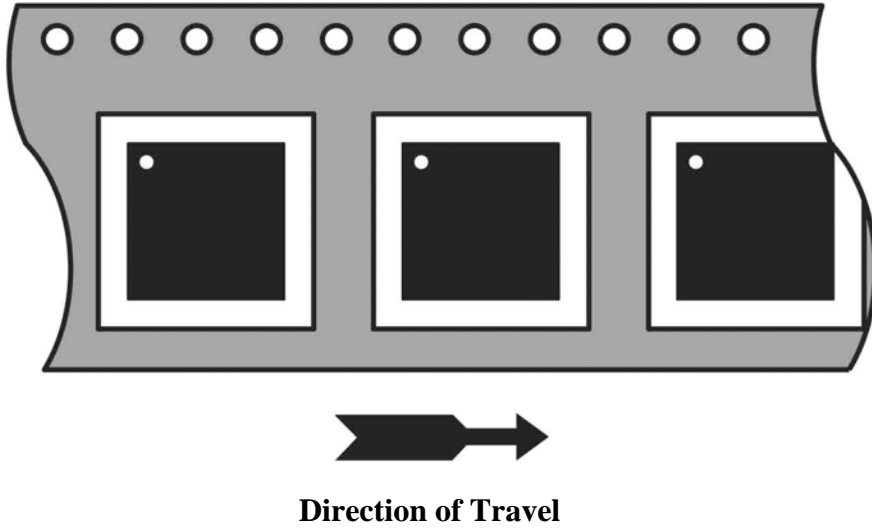
BOTTOM VIEW



SIDE VIEW

Note: All dimensions are in mm

TAPE & REEL PACKAGING
MLP 8 2x2mm



Package	Suffix	Reel Diameter	Quantity	Carrier Tape Width	Carrier Tape Pitch
MLP 8 (2x2mm)	R1	7"	1000	8mm	4mm
	R2	13"	2500	8mm	4mm

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