

AZP51

AZP52

AZP53

AZP54

Very Low Phase Noise Sine Wave/CMOS to LVPECL Buffer/Divider

PACKAGE AVAILABILITY

FEATURES

- 3.0 to 3.6 V operating supply range
- LVPECL Outputs
- Optimized for Low Phase Noise
- High Bandwidth to >800 MHz
- QFN 8 (1.5x1.5 mm) or SON 8 (1.5x1.0 mm) package
- Robust ESD Protection
HBM: >5 kV V_{DD} , >4 kV Q/Q, all other pins >2 kV
CDM: >2 kV
- S-Parameter (.s1p) and IBIS Model Files Available on Arizona Microtek Website

| BASE PART | PACKAGE | PART NO. | MARKING | NOTES |
|-----------|--|----------|-------------------|-------|
| AZP51 | SC-70 Green / RoHS Compliant / Lead (Pb) Free | AZP51SG | B<Date Code> | 1,4,6 |
| AZP52 | SC-70 Green / RoHS Compliant / Lead (Pb) Free | AZP52SG | C<Date Code> | 2,4,6 |
| AZP53 | QFN 8 (1.5x1.5 mm) Green / RoHS Compliant / Lead (Pb) Free | AZP53PG | D3 <Date Code> | 3,4,6 |
| | SON 8 (1.5x1.0 mm) Green / RoHS Compliant / Lead (Pb) Free | AZP53QG | D<Date Code> | 3,4,6 |
| AZP54 | SOT-23 Green / RoHS Compliant / Lead (Pb) Free | AZP54VG | D4<Date Code> | 1,4,6 |

- 1 $\div 1$
- 2 $\div 2$
- 3 $\div 1, \div 2$
- 4 Add R1 at end of part number for 7 inch, R2 for 13 inch Tape & Reel.
- 5 Date code format: "Y" for year followed by "WW" for week.
- 6 See Arizona Microtek web site for date code format.

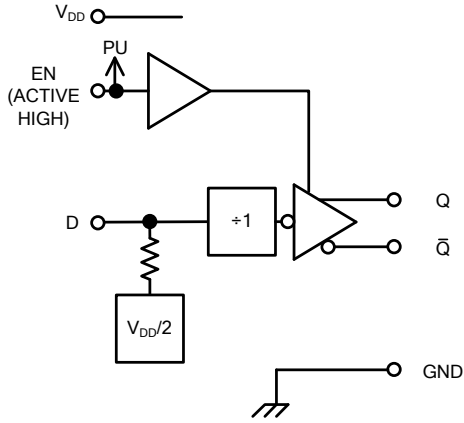
DESCRIPTION

The AZP51 series parts are sine wave/CMOS to LVPECL buffers optimized for low phase noise. They are particularly useful in converting crystal or SAW based oscillator outputs into LVPECL outputs. The AZP52 divides by 2, and the AZP53 includes selectable $\div 1, \div 2$ modes to provide better frequency range coverage when using a SAW based oscillator.

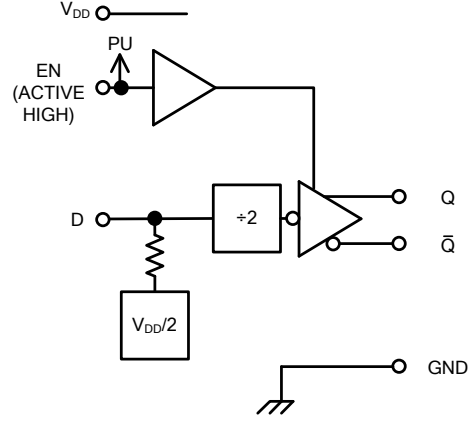
The D input is internally biased to $V_{DD}/2$. A sine wave input at least 750 mv p-p ensures the parts meet AC specifications. This input (D) should be capacitively coupled from the oscillator stage for best output duty cycle.

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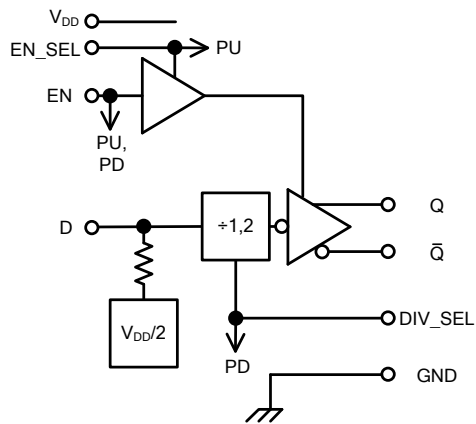
BLOCK DIAGRAMS



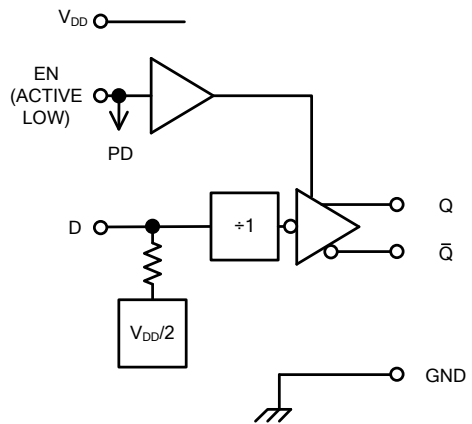
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SIGNAL DESCRIPTION

| PIN/PAD | FUNCTION |
|-----------------|----------------------------|
| D | Sine or CMOS Input |
| Q,Q | LVPECL Outputs |
| EN | Output Enable |
| DIV_SEL | Divide Select (AZP53 only) |
| EN_SEL | Enable Select (AZP53 only) |
| V _{DD} | Positive Supply |
| GND | Negative Supply (Ground) |

DIV-SEL OPERATION

| PART NUMBER | DIV-SEL | DIVIDE RATIO |
|----------------|-------------------------|--------------|
| AZP51 AZP54 | - ² | ÷1 |
| AZP52 | - ² | ÷2 |
| AZP53 | NC ¹ ,L H | ÷1 ÷2 |

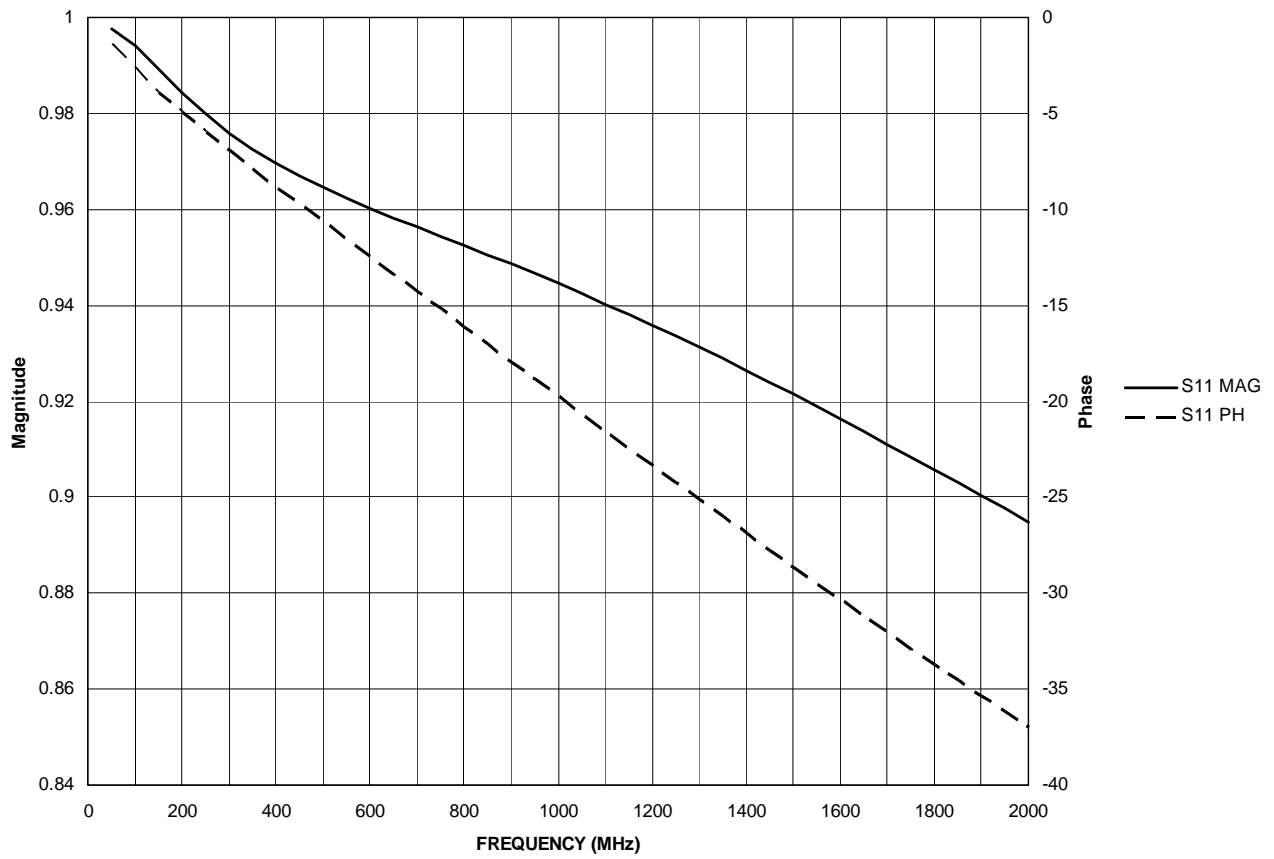
1. NC – no connection.
2. Internally connected.

FUNCTIONAL OPERATION

| PART NUMBER | INPUTS | | | EN LOGIC | EN PULLUP/ PULLDOWN | OUTPUTS | |
|----------------|---------------------|---------------------|----------------|--------------------------|------------------------|----------------|----------------|
| | EN_SEL ⁷ | EN | D | | | Q | Q |
| AZP51 AZP52 | - ² | NC ¹ , H | L | Active High ⁴ | Pullup | L ⁸ | H ⁸ |
| | | | H | | | H ⁸ | L ⁸ |
| | | L | X ⁵ | | | Z ⁶ | Z ⁶ |
| AZP53 | NC ¹ , H | NC ¹ , L | L | Active Low ³ | Pulldown | L ⁸ | H ⁸ |
| | | | H | | | H ⁸ | L ⁸ |
| | | | X ⁵ | | | Z ⁶ | Z ⁶ |
| | L | NC ¹ , H | L | Active High ⁴ | Pullup | L ⁸ | H ⁸ |
| | | H | H ⁸ | | | L ⁸ | |
| | L | X ⁵ | Z ⁶ | | | Z ⁶ | |
| AZP54 | - ² | NC ¹ , L | L | Active Low ³ | Pulldown | L | H |
| | | | H | | | H | L |
| | | | X ⁵ | | | Z ⁶ | Z ⁶ |

1. NC – no connection.
2. Internally tied, no pin.
3. Active Low: Output enabled when EN low, Tri-state when EN high.
4. Active High: Output enabled when EN high, Tri-state when EN low.
5. X – Don't care.
6. Z – High impedence.
7. EN_SEL input has an internal pullup.
8. ÷1 mode only.

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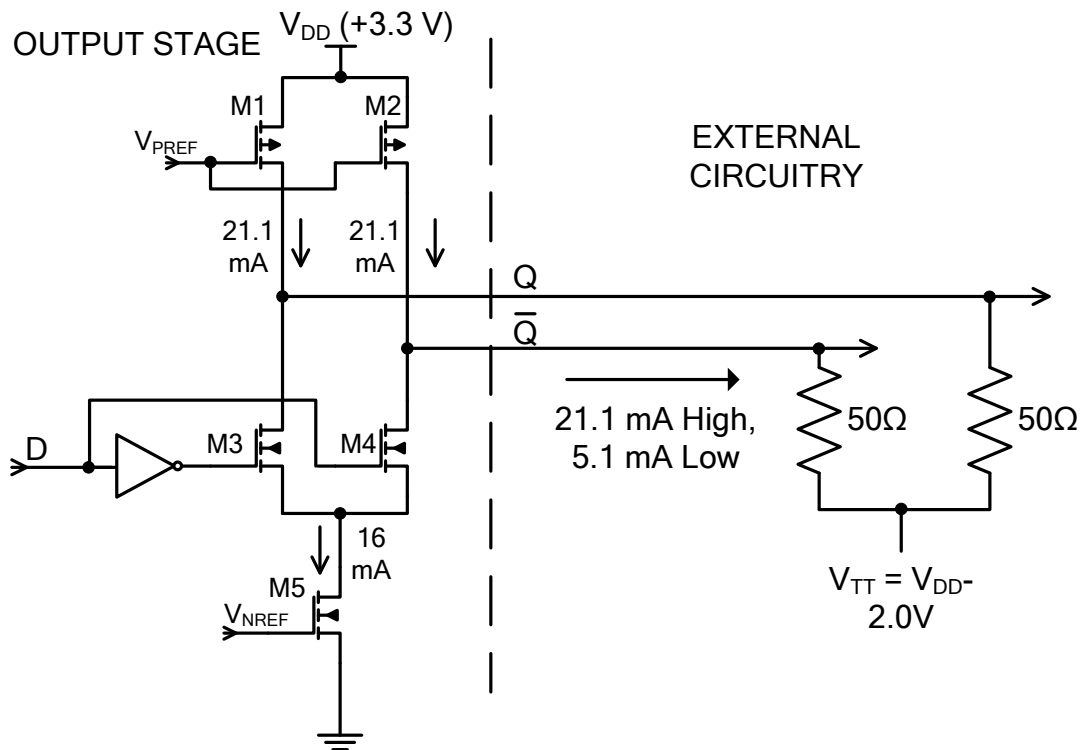
S11, D input, ÷1 and ÷2 modes

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Output Termination Techniques

The LVPECL compatible output stage of the AZP51 series parts uses a current drive topology to maximize switching speed as illustrated below. Two current source PMOS transistors (M1-M2) feed the output pins. M5 is an NMOS current source which is switched by M3 and M4. When M4 is on, M5 takes current from M2. This produces an output current of 5.1 ma (low output state). M3 is off, and the entire 21.1 ma flows through the output pin. The associated output voltage swings match LVPECL levels when external 50Ω resistors terminate the outputs.

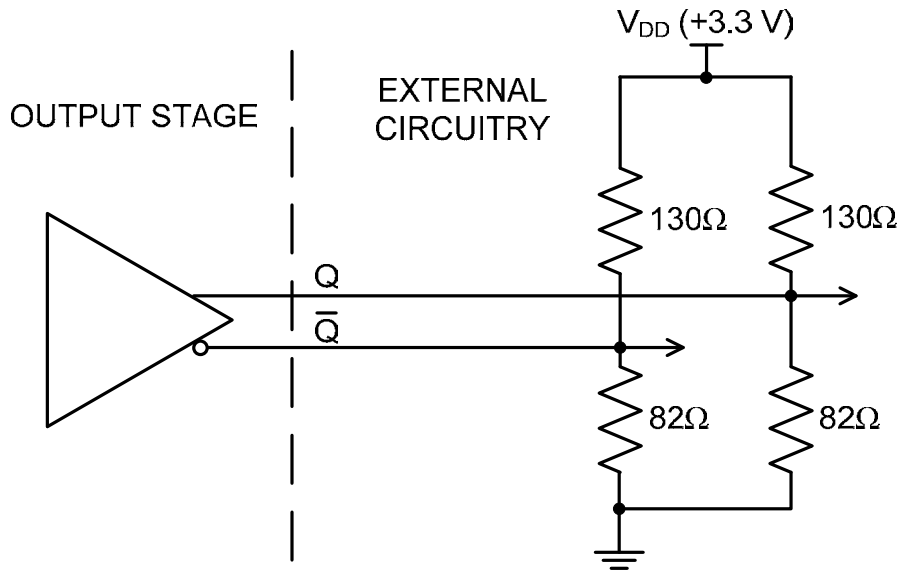
Both Q and \bar{Q} should always be terminated identically to avoid waveform distortion and circulating current caused by unsymmetrical loads. This rule should be connected between the outputs and $V_{DD}-2.0V$.



DUAL SUPPLY LVPECL OUTPUT TERMINATION

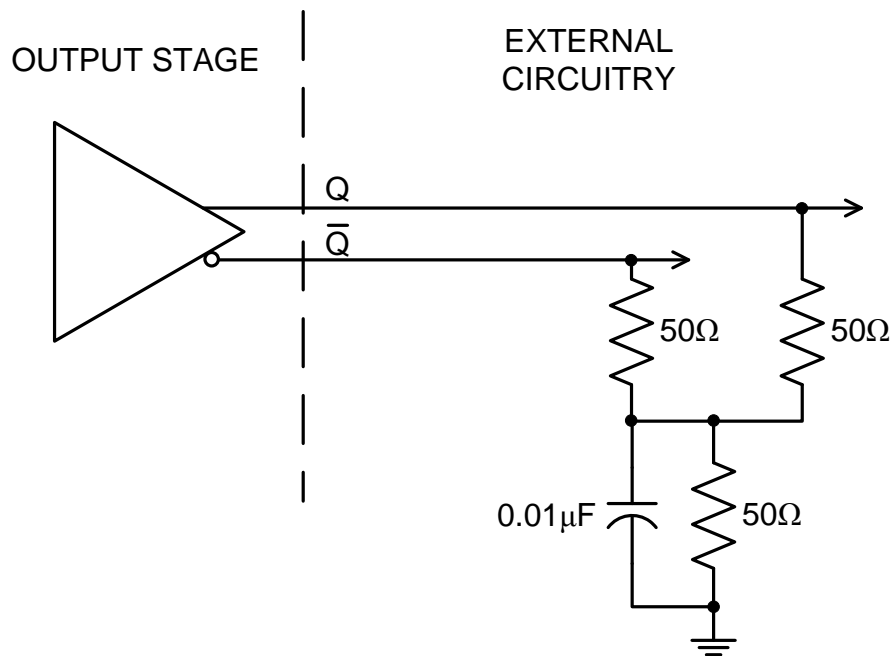
The standard LVPECL loads are a pair of 50Ω resistors connected between the outputs and $V_{DD}-2.0V$. The resistors provide both the DC and the AC loads, assuming 50Ω interconnects. This technique requires an additional supply, which may not be available in some applications. Another termination variant eliminates the need for the additional supply.

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FOUR RESISTOR TERMINATION

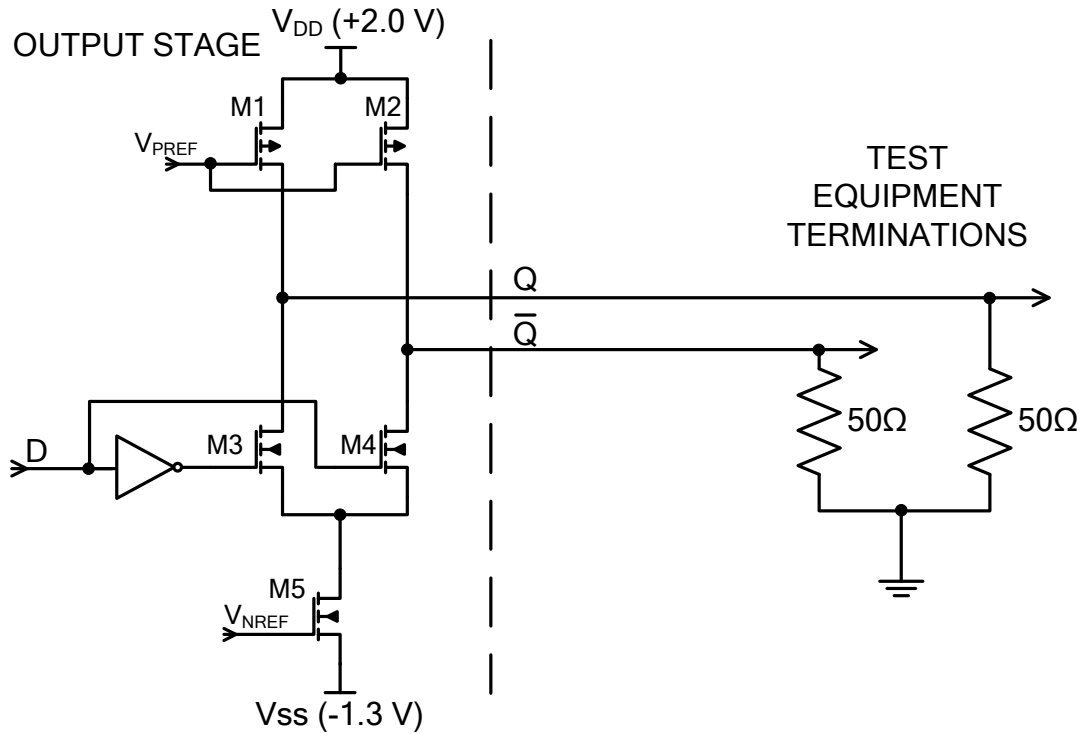
Alternately three resistors and one capacitor accomplish the same termination and reduce power consumption.



THREE RESISTOR TERMINATION

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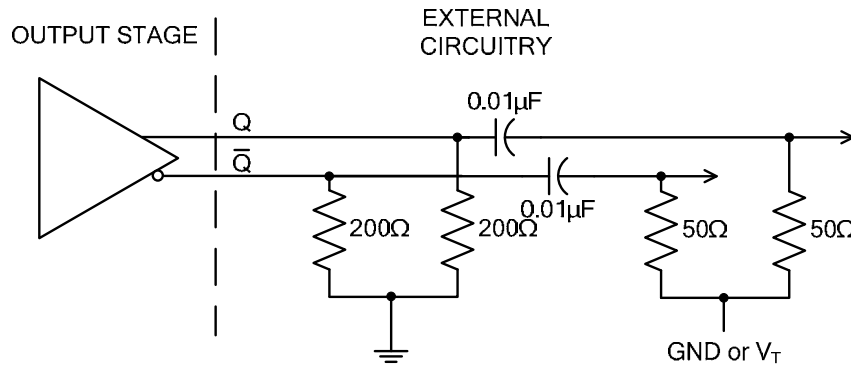
Arizona Microtek's evaluation board EBP53 provides the most convenient way to test and prototype AZP51 series circuits. Built for the AZP53Q 1.5x1.0 mm package, it is designed to support both dual and single supply operation. Dual supply operation ($V_{DD}=+2.0V$, $V_{SS}=-1.3V$) enables direct coupling to 50Ω time domain test equipment.



SPLIT SUPPLY LVPECL OUTPUT TERMINATION

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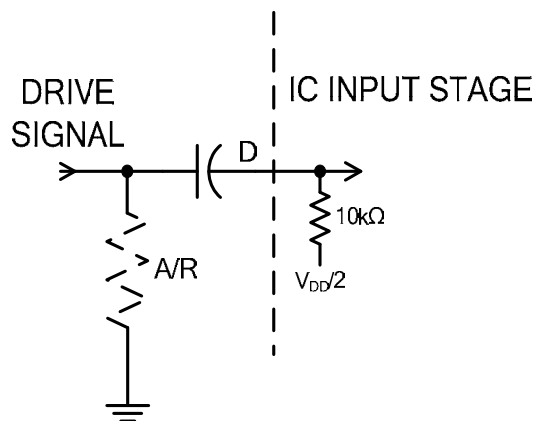
Clock applications or phase noise/frequency domain testing scenarios typically require AC coupling. The figure below shows the AC coupling technique. The 200Ω resistors form the required DC loads, and the 50Ω resistors provide the AC termination. The parallel combination of the 200Ω and 50Ω resistors results in a net 40Ω AC load termination. In many cases this will work well. If necessary, the 50Ω resistors can be increased to about 56Ω. Alternately, bias tees combined with current setting resistors will eliminate the lowered AC load impedance. The 50Ω resistors are typically connected to ground but can be connected to the bias level needed by the succeeding stage.



AC TERMINATION

Input Termination

The input pin bias is $V_{DD}/2$ fed through an internal 10kΩ resistor. For clock applications, the input signal should be AC coupled into the D input to maintain a 50% duty cycle on the outputs. The input can be driven to any voltage between 0V and V_{DD} without damage or waveform degradation.



INPUT INTERNAL TERMINATION

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Absolute Maximum Ratings are those values beyond which device life may be impaired.

| Symbol | Characteristic | Rating | Unit |
|------------------|-----------------------------|------------------------------|------|
| V _{DD} | Power Supply | 0 to +5.5 | Vdc |
| V _I | Input Voltage | -0.5 to V _{DD} +0.5 | Vdc |
| T _A | Operating Temperature Range | -40 to +85 | °C |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |

DC Characteristics (V_{DD} = 3.0V to 3.6V unless otherwise specified, T_A = -40 to 85 C)

| Symbol | Characteristic | Conditions | Min | Typ | Max | Unit | |
|-------------------|--|--|------------------------|-------|-----|-------|---|
| V _{OH} | Output HIGH Voltage ¹ | -40 C | V _{DD} = 3.3V | 2.05 | | 2.415 | V |
| | | 25 C | | 2.05 | | 2.480 | |
| | | 85 C | | 2.05 | | 2.540 | |
| V _{OL} | Output LOW Voltage ¹ | -40 C | V _{DD} = 3.3V | 1.365 | | 1.615 | V |
| | | 25 C | | 1.430 | | 1.680 | |
| | | 85 C | | 1.490 | | 1.740 | |
| I _Z | Output Leakage Current, Tri-state ² | EN=Disable ³ | -10 | | 10 | μA | |
| V _{IH} | High Level Input Voltage | EN_SEL ⁵ | 2.0 | | | V | |
| V _{IL} | Low Level Input Voltage | DIV_SEL ⁵ EN | | | 0.8 | V | |
| I _{PU} | Pullup Current | EN_SEL ⁵ | | 2.2 | | μA | |
| I _{PD} | Pulldown Current | DIV_SEL ⁵ | | -2.2 | | μA | |
| I _P | Pullup/Pulldown Current ⁴ | EN | | ±2.2 | | μA | |
| R _{BIAS} | Bias Resistor | D Input to Internal V _{DD} /2 Reference | | 10k | | Ω | |
| I _{DD} | Power Supply Current | | | 22 | 35 | mA | |
| I _{DDZ} | Power Supply Current – Outputs Tri-state ¹ | D Input ≤ V _{IL} EN=Disable ³ | | | 8 | mA | |

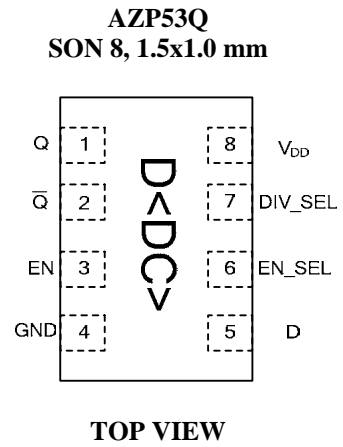
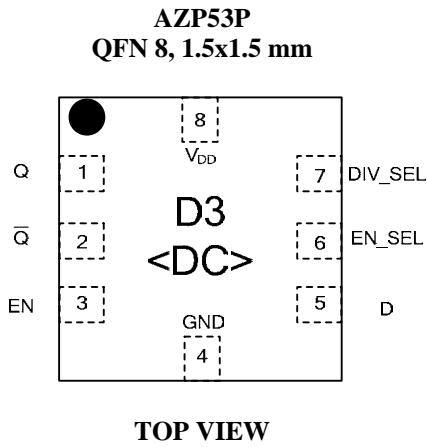
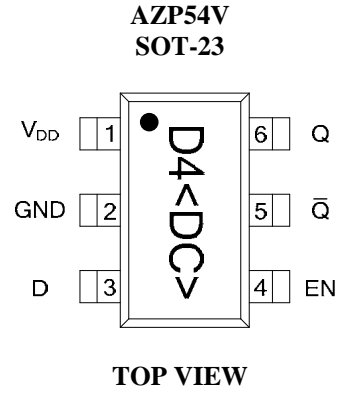
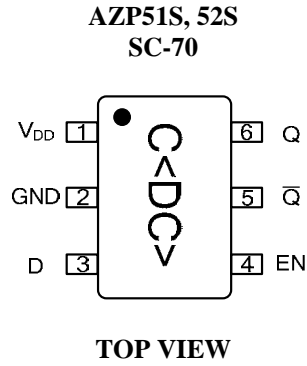
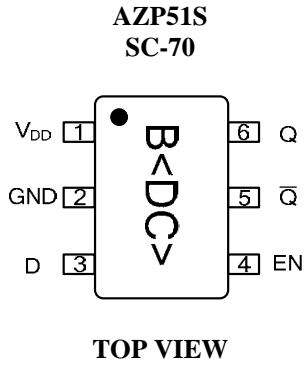
1. Specified with outputs terminated through 50Ω resistors to V_{DD} - 2V or Thevenin equivalent.
2. Measured at Q/Q pins.
3. See functional table for disable state definition.
4. See functional table for pullup/pulldown mode selection.
5. AZP53 only.

AC Characteristics (V_{DD} = 3.0V to 3.6V, T_A = -40 to 85 C)

| Symbol | Characteristic | | | Unit |
|---------------------------------|---|-----|-----------------|------------|
| | | Min | Max | |
| t _r / t _f | Output Rise/Fall ^{1,2} (20% - 80%) | 80 | 250 | ps |
| f _{MAX} | Maximum Input Frequency – Sine wave ² ÷1 ÷2 | | 800 1300 | MHz |
| V _{INMAX} | Maximum Recommended Input Signal | | V _{DD} | V p-p |
| V _{INMIN} | Minimum Recommended Input Signal | 0.2 | | V p-p |
| n _p | Phase Noise ^{1,2} 1 MHz offset | | -165 | dBc/ Hz |

1. Specified with outputs terminated through 50Ω resistors to V_{CC} - 2V or Thevenin equivalent.
2. 1.5 v p-p sine wave input, AC coupled to D pin.

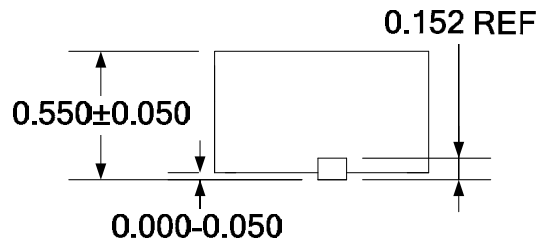
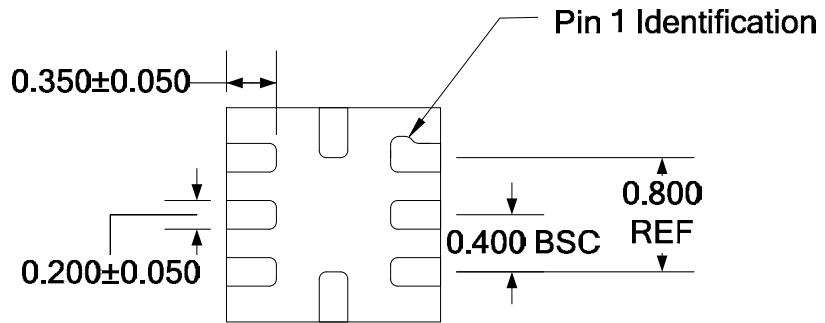
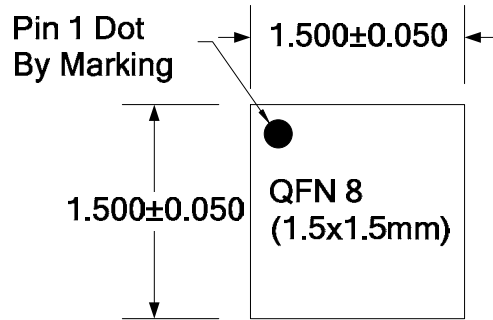
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<DC> = Date Code

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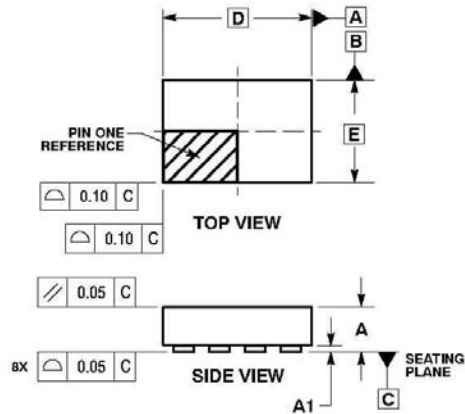
PACKAGE DIAGRAM
P – QFN 8 1.5x1.5mm



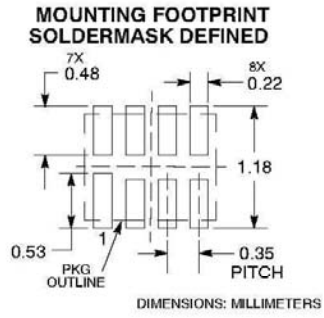
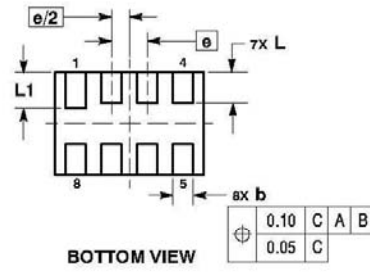
Note: All dimensions are in mm

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**PACKAGE DIAGRAM
 Q – SON 8 1.5x1.0mm**

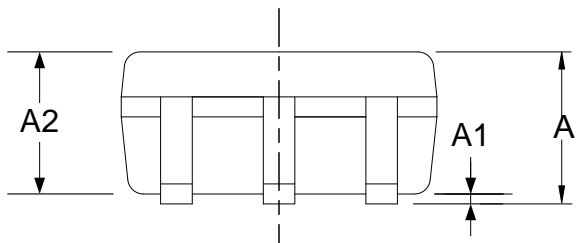
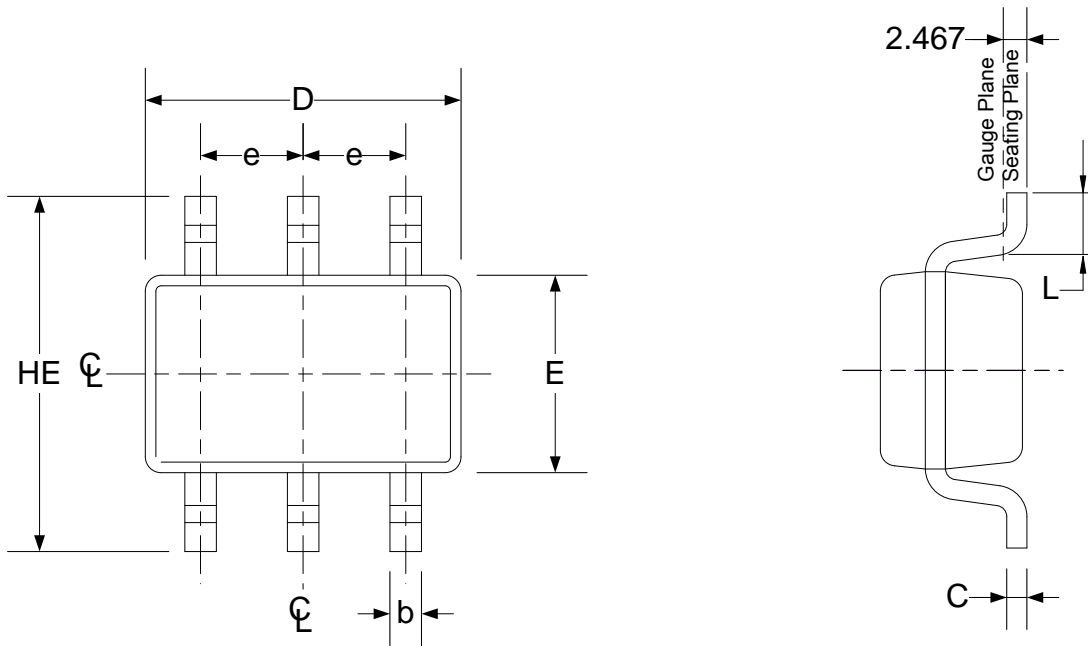


| MILLIMETERS | | |
|-------------|----------|------|
| DIM | MIN | MAX |
| A | --- | 0.40 |
| A1 | 0.00 | 0.05 |
| b | 0.15 | 0.25 |
| D | 1.50 BSC | |
| E | 1.00 BSC | |
| e | 0.35 BSC | |
| L | 0.25 | 0.35 |
| L1 | 0.30 | 0.40 |



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**PACKAGE DIAGRAM
 S – SC-70 6L**

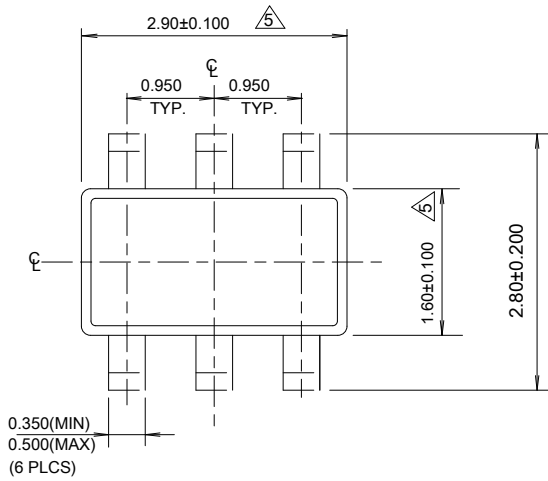


NOTE:
 1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & GATE BURR.

| SYMBOL | MIN | MAX |
|--------|----------|------|
| E | 1.15 | 1.35 |
| D | 1.85 | 2.25 |
| HE | 2.00 | 2.30 |
| A | 0.80 | 1.00 |
| A2 | 0.80 | 0.91 |
| A1 | 0.00 | 0.09 |
| e | 0.65 BSC | |
| b | 0.15 | 0.30 |
| c | 0.08 | 0.25 |
| L | 0.21 | 0.41 |

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PACKAGE DIAGRAM
V – SOT-23 6L

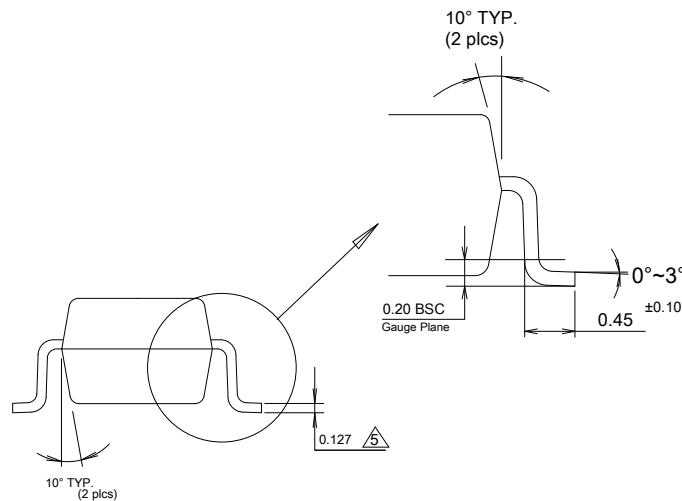
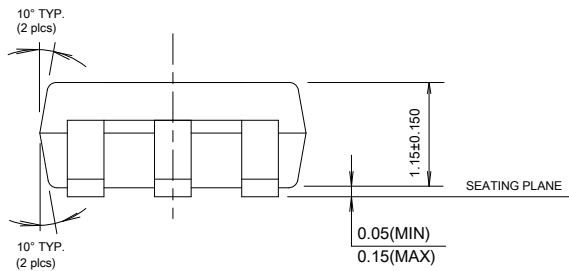


NOTE:

1. Dimensions and tolerances are as per ANSI Y14.5M, 1982.
2. Package surface to be matte finish VDI 11~13.
3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
4. The footlength measuring is based on the gauge plane method.

$\triangle 5$ Dimension are exclusive of mold flash and gate burr.

$\triangle 6$ Dimension are exclusive of solder plating.



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