

# AZ12010

## Multiply by 16, 32 Phase-Locked Loop Clock Generator

### FEATURES

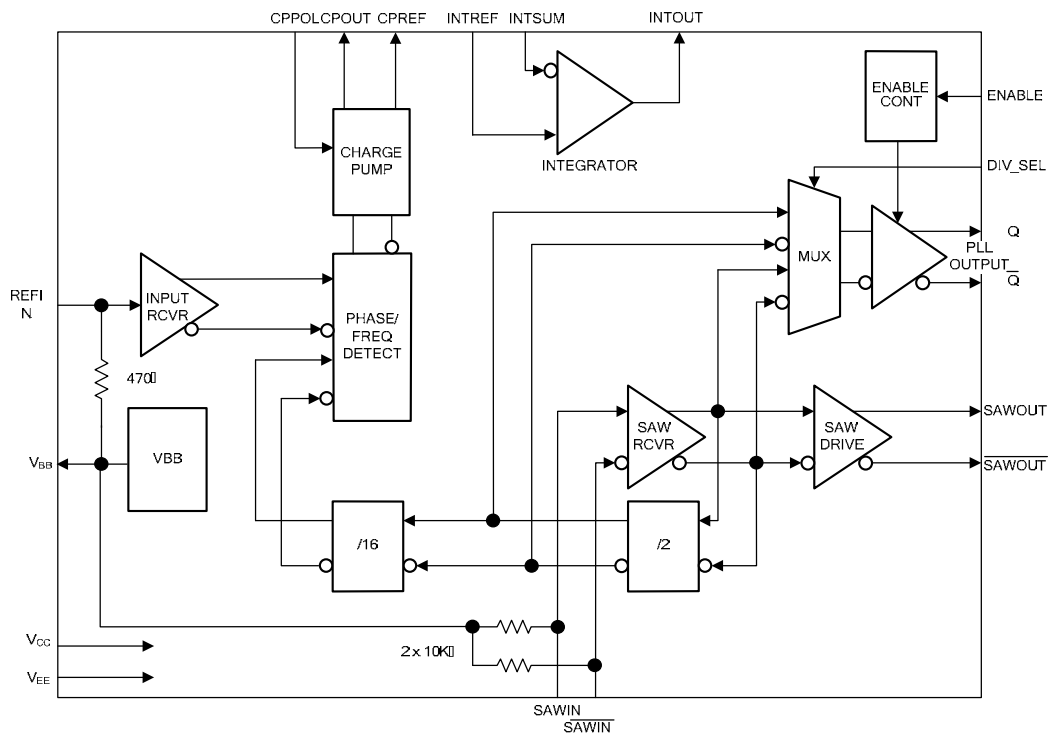
- Differential Inputs/Outputs for External Voltage Controlled SAW Oscillator
- Optional Internal Crystal Oscillator Driver
- Internal Edge-Matching Phase/Frequency Detector
- Internal Charge-Pump/Integrator Amplifier
- RF Bipolar Design for Low Phase Noise
- Available in a 3x3 mm MLP Package

### PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING	NOTES
MLP 16 (3x3) Green / RoHS Compliant / Lead (Pb) Free	AZ12010ALG	AZ12010A+ <Date Code>	1,2
MLP 16 (3x3) Green / RoHS Compliant / Lead (Pb) Free	AZ12010BLG	AZ12010B+ <Date Code>	1,2

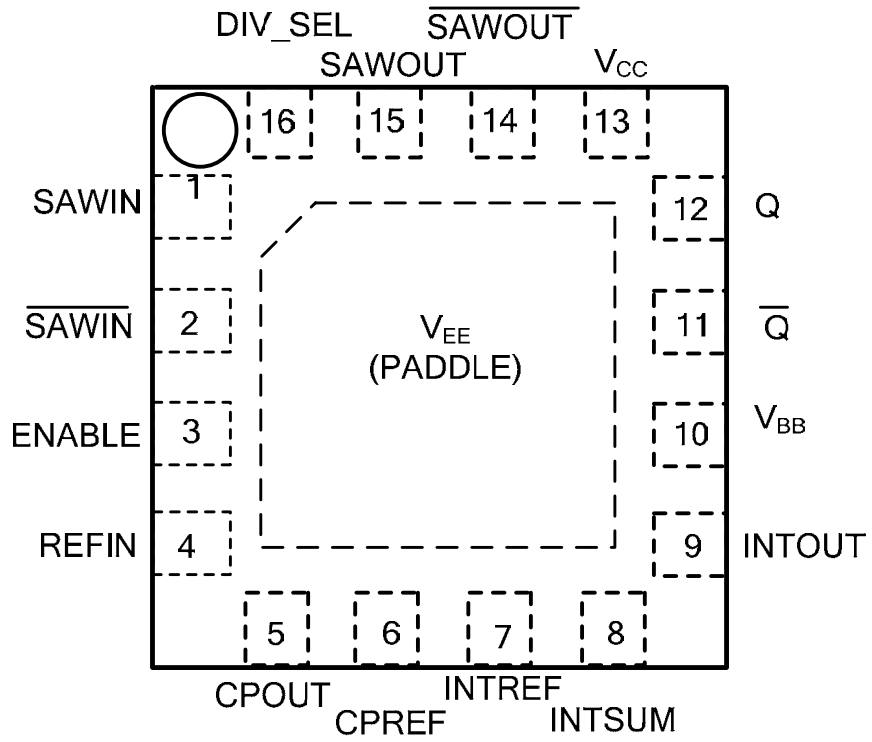
- 1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
- 2 Date code format: "YY" for year followed by "WW" for week.

### DESCRIPTION



The AZ12010 contains all of the functional elements necessary to implement a Phase-Locked Loop for clock multiplication at frequencies up to 800 MHz. A fixed 32 times multiplication allows the use of low cost crystals or a low frequency reference signal. The output can be divided by two for 16 times net multiplication. The VCISO is differentially or single-ended driven using the chip CML SAW outputs. The dynamic properties of the PLL are under the control of the user through selection of the desired external components.

**AZ12010**



**3X3 MLP 16 PACKAGE**

**AZM12010A: CPPOL pulled High**

**AZM12010B: CPPOL pulled Low**

## AZ12010 FUNCTIONAL PIN/PAD DESCRIPTIONS

Name	Functional Description	Logic Level
REFIN	<b>Reference Frequency Input</b> This pin/pad includes an on-chip 470 $\Omega$ pull down resistor to $V_{BB}$ . The input from the reference circuit should be AC coupled.	
CPREF	<b>Charge Pump Reference Output</b> The pin/pad voltage is nominally 1.2 volts below $V_{CC}$ .	
CPOUT	<b>Charge Pump Output</b> The charge pump output voltage is $V_{CPREF} \pm 0.3V$ during a phase correction pulse. When there is no correction pulse the output goes high impedance.	
CPPOL	<b>Charge Pump Polarity</b> When this pin/pad is pulled high the PLL operates with a VCISO circuit exhibiting negative pulling slope (the VCISO frequency goes down when the control voltage goes up). When this pin/pad is pulled low (AZM12010B) the PLL operates with a VCISO circuit exhibiting positive pulling slope (the VCISO frequency goes up when the control voltage goes up).  If the pin/pad is left open (AZM12010A), an internal pullup resistor selects negative pulling slope mode.	LVC MOS LVTTL
INTREF	<b>Integrator Reference Input</b> This pin/pad should be connected to CPREF through a bias current cancellation network	
INTSUM	<b>Integrator Summing Junction</b> This pin/pad is the summing junction for the integrator amplifier	
INTOUT	<b>Integrator Output</b>	
SAWIN SAWIN	<b>SAW Amplifier Inputs</b> If only one input is used (Single-ended VCISO), the unused input should be bypassed with a capacitor to $V_{BB}$ .	
SAWOUT SAWOUT	<b>SAW Amplifier Outputs</b> These are open collector outputs for driving the VCISO device. Operating at nominally 9 ma, external pullup resistors must be connected between these pins/pads and $V_{CC}$ . If only one output is used, the other output should be connected to $V_{CC}$ through a 50 $\Omega$ resistor.	CML (Analog)
ENABLE	<b>PLL Output Enable</b> The Q and Q outputs are enabled when this pin/pad is pulled high. When this pin/pad is low, the Q output is high, and the Q output is low. If the pin/pad is left open, an internal pullup resistor enables the outputs.	LVC MOS LVTTL
DIV_SEL	<b>Divide Select</b> When this pin/pad is high, the Q and Q outputs are divided by one from the SAW device. When it is low, the Q and Q outputs are divided by two from the SAW device. If the pin/pad is left open, an internal pullup resistor selects the divide by one mode.	LVC MOS LVTTL
Q Q	<b>Clock Output</b> These pin/pads are the main clock output. When ENABLE is low, the outputs are disabled with Q high and Q low.	PECL
$V_{BB}$	<b>Reference Voltage Output</b> This pin/pad is used to bias the REFIN signal. It must be bypassed externally to the $V_{EE}$ pins/pads with a 0.01 $\mu F$ capacitor.	
$V_{CC}$	<b>Positive Supply</b> +3.0 to +3.6 V	
$V_{EE}$	<b>Negative Supply</b> Ground	

**Absolute Maximum Ratings are those values beyond which device life may be impaired.**

Symbol	Characteristic	Rating	Unit
$V_{CC}$	Power Supply ( $V_{EE} = GND$ )	0 to +6.0	Vdc
$V_I$	Input Voltage ( $V_{EE} = GND$ )	0 to +6.0	Vdc
$I_{OUT}$	PECL Output Current — Continuous — Surge	50 100	mA
$T_A$	Operating Temperature Range	-40 to +85	$^{\circ}C$
$T_{STG}$	Storage Temperature Range	-65 to +150	$^{\circ}C$

# AZ12010

## AZ12010 DC CHARACTERISTICS ( $V_{CC} = +3.0$ to $+3.6$ V, $V_{EE} = \text{GND}$ )

Symbol	Characteristic	-40°C		0°C		25°C			85°C		Unit
		Min	Max	Min	Max	Min	Typ	Max	Min	Max	
$V_{BB}$	Reference Voltage	$V_{CC}$ -1.38	$V_{CC}$ -1.26	$V_{CC}$ -1.38	$V_{CC}$ -1.26	$V_{CC}$ -1.38	$V_{CC}$ -1.31	$V_{CC}$ -1.26	$V_{CC}$ -1.38	$V_{CC}$ -1.26	V
$R_{REF}$	REFIN Pull-Down resistor to $V_{BB}$						470				$\Omega$
$R_{SAW}$	SAWIN, SAWIN Pull-Down resistor to $V_{BB}$						10K				$\Omega$
$V_{HCTL}$	High level integrator output	$V_{CC}$ -1.0		$V_{CC}$ -1.0		$V_{CC}$ -1.0			$V_{CC}$ -1.0		V
$V_{LCTL}$	Low level integrator output		0.5		0.5			0.5		0.5	V
$V_{OH}$	Output HIGH Voltage <sup>1</sup> Q, Q	$V_{CC}$ -1085	$V_{CC}$ -880	$V_{CC}$ -1025	$V_{CC}$ -880	$V_{CC}$ -1025	$V_{CC}$ -955	$V_{CC}$ -880	$V_{CC}$ -1025	$V_{CC}$ -880	mV
$V_{OH}$	Output HIGH Voltage <sup>2</sup> SAWOUT, SAWOUT	$V_{CC}$ -10	$V_{CC}$	$V_{CC}$ -10	$V_{CC}$	$V_{CC}$ -10		$V_{CC}$	$V_{CC}$ -10	$V_{CC}$	mV
$V_{OL}$	Output LOW Voltage <sup>1</sup> Q, Q	$V_{CC}$ -1830	$V_{CC}$ -1555	$V_{CC}$ -1810	$V_{CC}$ -1620	$V_{CC}$ -1810	$V_{CC}$ -1705	$V_{CC}$ -1620	$V_{CC}$ -1810	$V_{CC}$ -1620	mV
$V_{OL}$	Output LOW Voltage <sup>2</sup> SAWOUT, SAWOUT	$V_{CC}$ -349	$V_{CC}$ -481	$V_{CC}$ -365	$V_{CC}$ -516	$V_{CC}$ -392	$V_{CC}$ -449	$V_{CC}$ -557	$V_{CC}$ -465	$V_{CC}$ -661	mV
$V_{IH}$	Input HIGH Voltage, LVCMOS/LVTTL EN, DIV_SEL	2.2	$V_{CC}$	2.2	$V_{CC}$	2.2		$V_{CC}$	2.2	$V_{CC}$	V
$V_{IL}$	Input LOW Voltage, LVCMOS/LVTTL EN, DIV_SEL	0.0	0.8	0.0	0.8	0.0		0.8	0.0	0.8	V
$I_{CC}$ ( $I_{EE}$ )	Power Supply Current		65		65	45	54	65		65	mA

1. Load is  $50\Omega$  to  $V_{CC}-2V$
2. Load is  $50\Omega$  to  $V_{CC}$

## AZ 12010 AC CHARACTERISTICS ( $V_{CC} = +3.0$ to $+3.6$ V, $V_{EE} = \text{GND}$ )

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$A_{PD}$	Phase Detector Gain					20.3					radians/V
$f_{VCO}$	External VSCO frequency			800			800			800	MHz
$t_r / t_f$	Output Rise & Fall Times (20% - 80%) Q, Q					120					ps
$a_v$	SAW Amplifier and Driver Gain at 622.08 MHz <sup>1</sup>	18	24.5	28	15.5	21	24.5	13.5	19	22.5	dB

1. Single Ended Input and Output, Driven from  $50\Omega$  backmatched source, Load  $50\Omega$  to  $V_{CC}$ .

**Loop Filter Design**

The combination of the phase detector, amplifier, VCO and divider form a second-order phase-locked loop. Proper selection of the loop components is important to obtain stable, low jitter operation.

The loop bandwidth (or natural frequency,  $\omega_n$ ) and damping factor ( $\zeta$ ) are the two major driving forces that define the loop's response to a disturbance. The value of  $\zeta$  is typically 0.7 to ensure the fastest step response consistent with no ringing. However in many oscillator application  $\zeta$  may be 3 or higher to provide further phase noise reduction.  $\omega_n$  is chosen as a compromise between settling time, VCO jitter and reference feedthrough. These values can be computed by the following equations:

$$\omega_n = \frac{1}{N} \sqrt{\frac{K_\phi K_{VCO}}{\tau_1}}$$

$$\zeta = \frac{\tau_2 \omega_n}{2}$$

$$\tau_1 = R_1 C_1$$

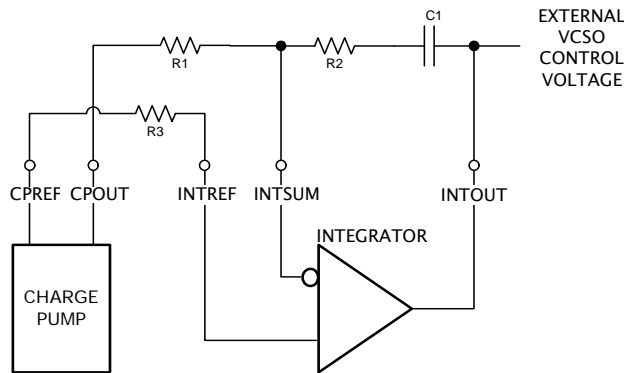
$$\tau_2 = R_2 C_1$$

$K_\phi$  = Phase Detector Gain (20.3 radians/V)

$K_{VCO}$  = VCO Gain (radians/sec/volt)

$N$  = Frequency Divisor value (32)

The component definitions are shown in the figure below. R3 should be equal to R1 to minimize integrator offsets.



**Figure 1 Charge Pump and Integrator**

Application Circuit

A typical application circuit is shown in Figure 2.

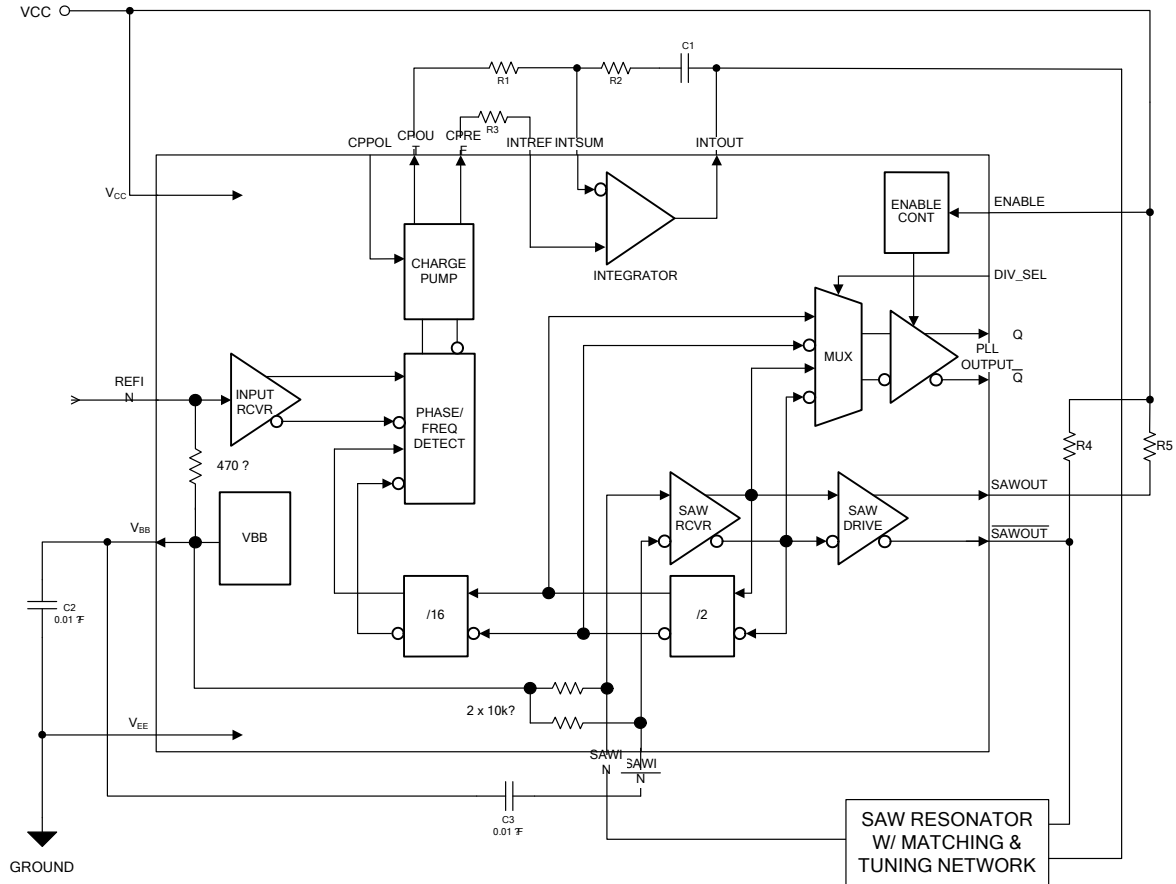
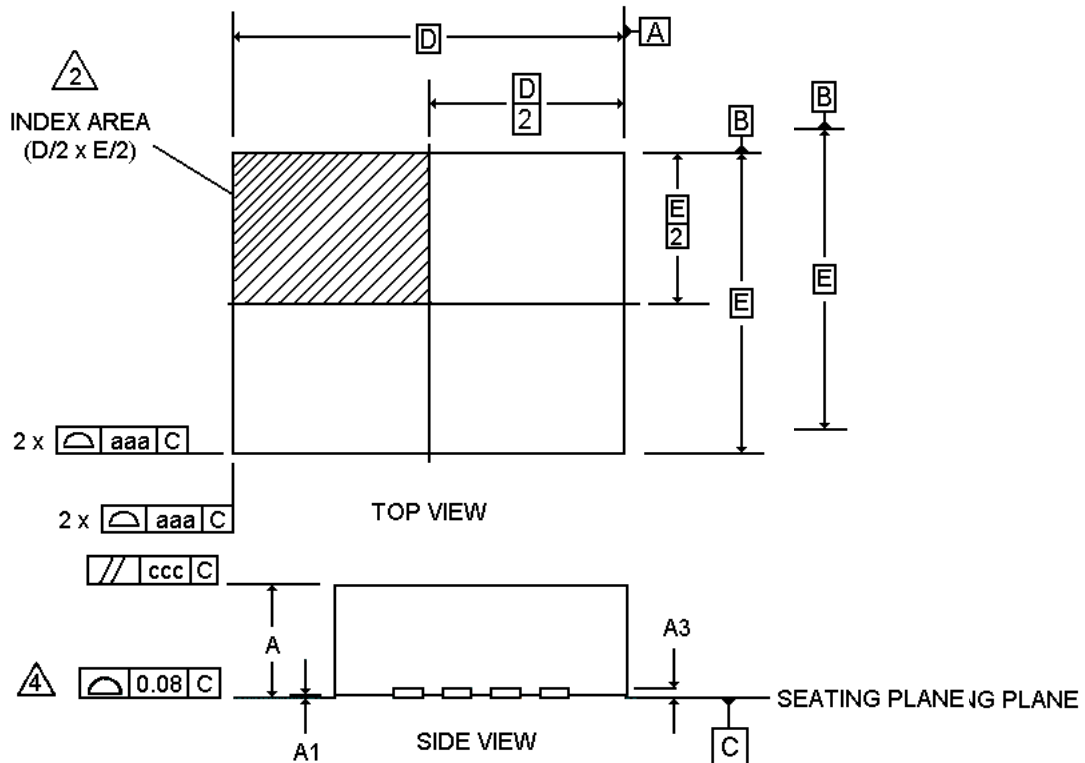


Figure 2. Typical Application, Always Enabled and Divide by One for Output

**PACKAGE DIAGRAM  
MLP 16**

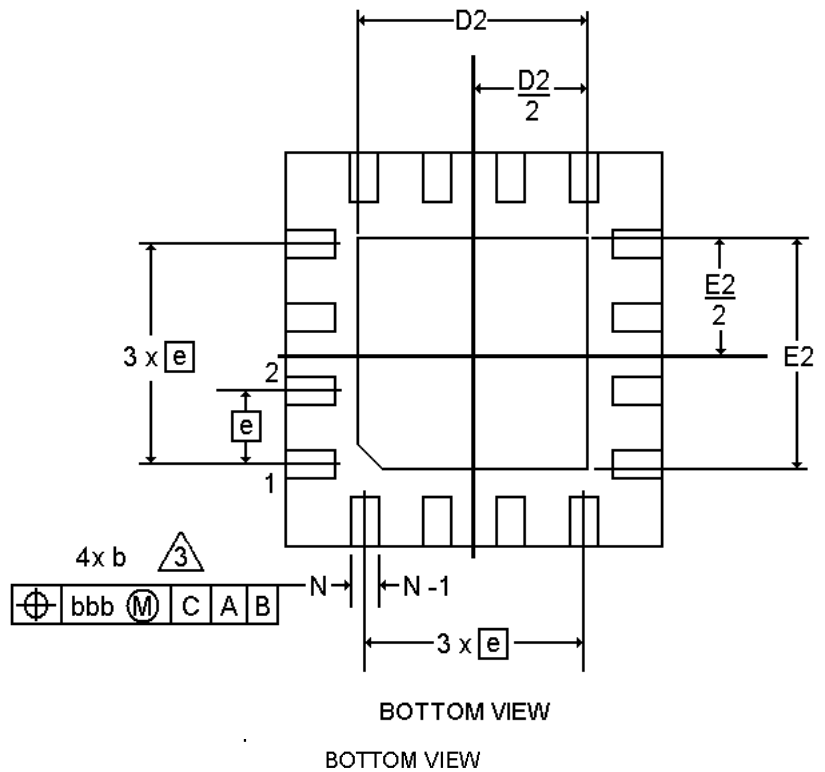


NOTES

NOTES

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
2. THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
3. DIMENSION *b* APPLIES TO METALLIZED PAD AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM PAD TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.10
A1	0.00	0.05
A3	0.25 REF	
<i>b</i>	0.225	0.275
D	2.90	3.10
D2	1.65	1.95
E	2.90	3.10
E2	1.65	1.95
<i>e</i>	0.50 BSC	
L	0.35	0.45
aaa	0.25	
bbb	0.10	
ccc	0.10	



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